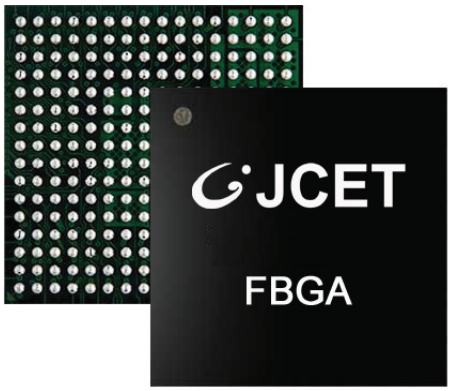
FBGA

Fine Pitch Ball Grid Array

Highlights

- Array molded, cost effective, space-saving package solution
- Available in 1.40mm (LFBGA), 1.20mm (TFBGA), 1.00mm (VFBGA), 0.80mm (WFBGA), 0.65mm (UFBGA) and and 0.50mm (XFBGA) maximum thickness
- Laminate substrate-based package which enables 1, 2, 3 and 4 layers of routing flexibility



Features

- Thin, lightweight, space-saving package
- Flexible body sizes range from 3 x 3mm to 23 x 23mm with square or rectangular body size options
- 0.40, 0.50, 0.65, 0.75, 0.80, 1.00mm ball pitch
- Eutectic & Pb free solder balls
- Green package available
- Multiple routing layers and dedicated ground/power planes available for improved electrical performance
- BT laminate materials (1, 2, 3 and 4 metal layers)
- JEDEC standard compliant

Applications

- Microprocessors/Controllers
- Wireless RF
- Analog
- ASIC
- Memory
- Simple PLDs
- Others

Description

BGA technology was first introduced as a solution for the increasingly high lead counts required for advanced semiconductors used in applications such as portable computers and wireless telecommunications. As the number of leads surrounding the ICs increased, high lead count packages experienced significant electrical shorting problems. BGA technology solves this problem by effectively creating leads on the bottom surface of the package in the form of small bumps or solder balls.

BGA packages can be used for high performance applications with high I/O connections and high thermal and electrical requirements. The characteristics of BGA packages make them suitable for a wide variety of devices used in computing platforms, networking, hand-held consumer products, wireless communications devices, video cameras, home electronic devices and game consoles.

We offer a range of BGA packages including the FBGA. The Fine Pitch Ball Grid Array (FBGA) is a laminate substrate-based chip scale package with plastic overmolded encapsulation and an array of fine pitch solder ball terminals. FBGA is a package that is widely used in space constrained applications such as mobile and handheld computing devices. FBGA's reduced outline and thickness and higher density options make it an ideal advanced technology packaging solution for high performance and/or portable applications.

Our FBGA is available in a broad range of JEDEC standard body sizes with LFBGA (<1.70mm [typically <1.40mm]), TFBGA (<1.20mm), VFBGA (<1.00mm), WFBGA (<0.80mm), UFBGA (0.65mm max.) and XFBGA (0.50mm max.) thickness. The use of the latest materials and advanced assembly infrastructure produce a reliable and cost effective package. Lead free and halogen free compatible material sets are available.

Specifications

Die Thickness	50-300µm (3-12mils)
Gold Wire	15-30µm (0.6/0.8/0.9/1.0/1.2mils) diameter
Pd/Cu Wire	15-25µm (0.6/0.7/0.8/1.0mils) diameter
Ag Wire	18-25µm (0.7/0.8/1.0mils) diameter
Mold Cap Thickness	0.25-1.22mm
Marking	Laser
Packing Options	JEDEC tray/tape & reel

Reliability

Moisture Sensitivity Level	JEDEC Level 2A, 260°C Reflow
Temperature Cycling	Condition C (–65°C to 150°C), 1000 cycles
High Temperature Storage	150°C, 1000 hrs
Pressure Cooker Test	121°C, 100% RH/2 atm, 168 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs
Unbiased HAST	130°C/85% RH/2 atm, 96 hrs

Thermal Performance θja (°C/W)

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Performance θja (C/W)
LFBGA	11 x 11 (2L)	144	4.5 x 4.5	34.1
LFBGA	15 x 15 (4L)	208	10.2 x 10.2	19.4

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-7) under natural convection as defined in JESD51-2.

Electrical Performance

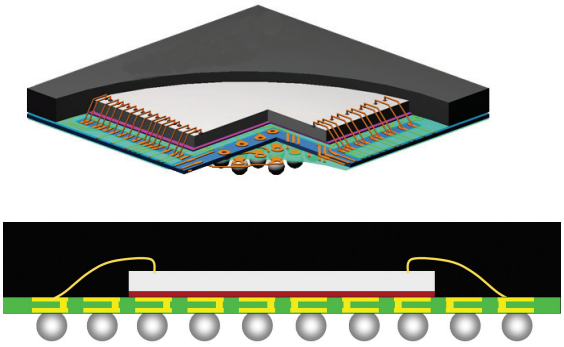
Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	34 - 119	1.30 - 4.55	0.26 - 2.28	0.25 - 0.95	0.06 - 0.42
Total (2L)	4 - 9	154 - 239	2.95 - 6.20	0.71 - 3.13	0.35 - 1.05	0.07 - 0.44
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (4L)	2 - 7	34 - 119	0.90 - 3.15	0.18 - 1.58	0.35 - 1.10	0.06 - 0.42
Total (4L)	4 - 9	154 - 239	2.55 - 4.80	0.63 - 2.43	0.45 - 1.20	0.07 - 0.44

Note: Results are simulated values per JEDEC EIA/JEP123 standards.

Cross Sections

FBGA



Package Configurations

Body Sizes (mm)	3x3 to 23x23 with square or rectangular body size options; Common body sizes: 5x10, 7x9, 8x10, 8x11, 8x12, 8x14, 10x12, 10x14, 13x13, 15x15, 16x16, 17x17
Ball Count	40 to 450
Ball Pitch (mm)	0.40 to 1.0
Typ. Pkg. Thickness	LFBGA: 1.70mm (1.40mm max. typical) TFBGA: 1.20mm max. VFBGA: 1.00mm max. WFBGA: 0.80mm max. UFBGA: 0.65mm max. XFBGA: 0.50mm max.

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