28nm CPI (Chip/Package Interactions) in Large Size eWLB (Embedded Wafer Level BGA) Fan-Out Wafer Level Packages

by

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***Abstract*— To meet the continued demand for form factor reduction and functional integration of electronic devices, Wafer Level Packaging (WLP) is an attractive packaging solution with many advantages in comparison with standard Ball Grid Array (BGA) packages. The advancement of fan-out WLP has made it a more promising solution as compared with fan-in WLP, because it can offer greater flexibility in enabling more IO's, multi-chips, heterogeneous integration and 3D SiP. In particular, Embedded Wafer Level BGA (eWLB) is a fan-out WLP solution which can enable applications that require higher input/output (I/O) density, smaller form factor, excellent heat dissipation, and thin package profile, and it has the potential to evolve in various configurations with proven integration flexibility, process robustness, manufacturing capacity and production yield. It also provides integration of multiple dies vertically and horizontally in a single package without substrates.**

For eWLB fan-out WLP, the structural design as well as selection of materials is very important in determining the process yield and long term reliability. Therefore it is necessary to investigate the key design factors affecting the reliability comprehensively. This work is focused on an experimental study on the chip-package interactions in 10x10~15x15mm 28nm eWLB fan-out WLP with multiple redistribution layers (RDLs). Standard JEDEC component and board level tests were carried out to investigate reliability, and both destructive and non-destructive analyses were performed to investigate potential structural defects. Electrical characterization was also studied for both simulation and experimental works. The influence of structural design on the package reliability will be demonstrated. Thermal characterization and thermo-mechanical simulation results will also be discussed.

Keywords-component; eWLB, FOWLP, CPI, Cu low-k device, 28nm, Reliability,

I. INTRODUCTION

The packaging technologies For advanced integrated circuits are mainly based on the area-array packages, or the flip chip solder interconnects. This type of first-level structure interconnects the side of the active device at the face-down silicon (Si) die via solder bumps on a multilayered organic substrate. The area array configuration has the ability to support the required input/output (I/O) pad counts and power distribution due to the improvement of the device density and performance[1]. The growth of microelectronic technology to meet various market demands requires innovative package technology. In turn, there is always the potential to encounter unexpected CPI challenges in semiconductor manufacturing. The ultimate goal of CPI work is to understand the structural integrity of a package through various reliability and stress tests as well as to monitor any potential manufacturing or reliability related failures[2]. As the industry faced several CPI related failures over the last decade, CPI qualification became one of the prerequisites for technology qualification before a product tape-out. Unfortunately, each package faces different challenges, so it is important to evaluate and qualify it independently. Firstly CPI challenges are to understand their origin and underlying contributing parameters. For example, the main CPI challenge for a wire bonding device comes from thermomechanical stress during the wire bond process on a bond pad in back-end-of-line (BEOL), while the biggest challenge for flip chip devices comes from the mismatch of the coefficient of thermal expansion (CTE) of the individual package components after chip attach[3]. These days the CPI challenges is very complex and needs extensive study and examination from various view angles with more complicated of advanced node device and new packaging solutions as shown Fig.1[4].

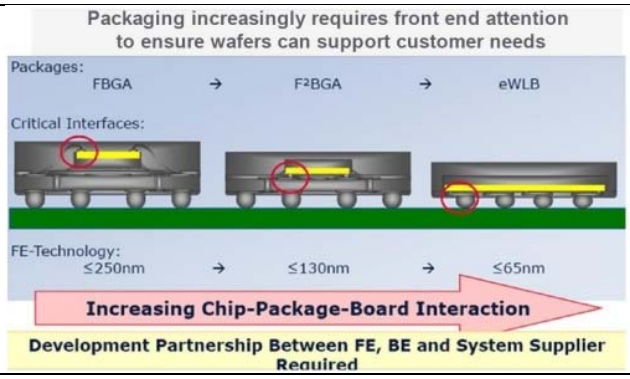

Figure 1. Packaging influences the front end [4].

For advanced silicon node chips, it is well known that the low-k layer is one of the weakest points from a CPI perspective. Therefore, the main areas of interest are low-k layers in the BEOL stack and solder joint domains, which is where the localized sub-models are focused. In general,

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based on these finite element analysis (FEA) simulation results, the BEOL stack with the highest CPI risk is chosen for package reliability testing using the CPI test vehicle (TV).
In this work, we assess production readiness for large body size multilayer RDL based eWLB packages through;

- Functional test of 28nm circuits
- Reliability test
- Electrical and thermal characterization
- Thermo-mechanical characterization and simulation

Advanced Wafer-Level Technology: eWLB/FOWLP

eWLB package technology is based on an embedded device technology with fan-out redistribution. The thin-film redistribution layer (RDL) of the eWLB enables very flexible and highly customizable package designs. The length of the redistribution lines is in the range of the die size[5].
eWLB has the ability to attain minimum interconnection length and excellent electrical performance. In a few cases, eWLB achieved a 20~40% reduction in package size and over 50% volume reduction as compared to other packaging solutions such as flipchip or wirebonding packages due to its slim and smaller form factor. For radio frequency (RF) and high-frequency microwave or mmWave devices, a significantly improvements in overall device performance was illustrated by eWLB, which showed less parasitic electrical interference.

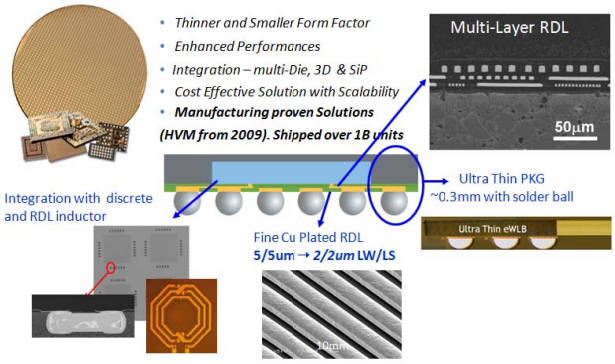


Figure 2. Key features of advanced eWLB/FO–WLP: Innovative and high performance solution of integration

II. EXPERIMENTAL WORKS

Test Vehicle Specification

The three different test vehicles were designed with 10x10-15x15mm package sizes and multi-layer RDL. And those test vehicles were assembled and packaged with the eWLB technology of advanced dielectric materials using low temperature curable process, as previously reported, for robust package reliability [5]. Table 1 and Fig. 3 show the package specification and design of each test vehicle.

Table 1. Test Vehicle Specification.

	TV-1	TV-2	TV-3
PKG Size	15x15mm	14x16mm	10x10 mm
Die Size	13x13mm	11x11mm	7x7 mm
Ball Pitch	400um	400um	400um
RDL Layers	3	2	2
Die Thickness	200um	150/2500/350um	150um
Package ball height/size	190um	110um	110um
PKG Thickness (Max.)	450um	200/300/400um	2000um

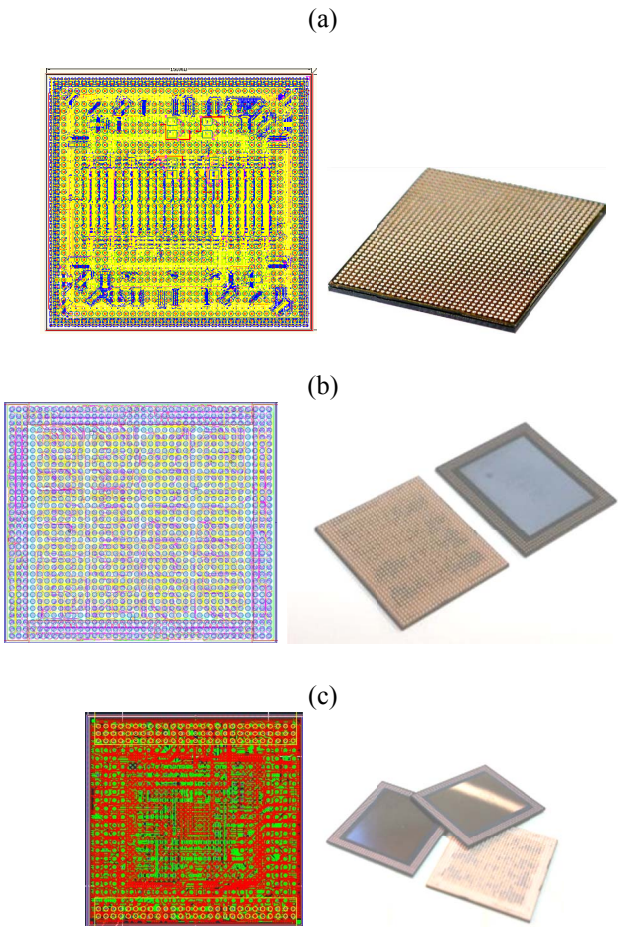


Figure 3. Test vehicles of 28nm CPI works; (a) TV-1 (b)TV-2 and (c)TV-3.

Reliability Test

For component level reliability tests, eWLB test vehicles were assembled with daisychain and electrical functional devices. Table 2 shows the package level reliability test conditions in this study.

All tested eWLB parts tested passed both JEDEC standard package level and board level reliability conditions successfully. eWLB with advanced dielectric materials passed JEDEC TC-B condition (-55/125°C) For temperature cycling (TC) reliability test. For thinner package of 200um body thickness, it passed 1000 cycles in TCoB. Even after 300 drops, no failure has recorded and drop reliability performance was robust

Table 2. Package & Board Level Reliability Results of eWLB with advanced dielectric material.

Test	Test Condition	Test Conditions
PC Pre-Cond	JEDEC J-STD-020	MSL1 24h bake @ 125°C 192h @ 30°C/60%RH Reflow simulation (3times) with Lead free profile Tmax=260°C
TC Temp. Cycling	JESD22-A104	Ta = -55/+125°C 1000 cycles
HTSL, High Temp. Storage Life	JESD22-A103	Ta=150°C 1000h
THS, Temp Humidity Storage	JESD22-A101	Ta=85°C, 85%RH 1000h without bias
TCoB	JESD22-A103	-40/125C, 500 cycles
Drop Test	JESD22-B111	1500G , 100 drops

Via Shape Simulation

RDL Via Shape Simulation

RDL via shape design is critical for interconnection with advanced node devices. In this study, the FEA approach is adopted to evaluate the effect of different RDL1 via interconnect structures on the thermomechanical stresses in BEOL layer in a semiconductor die of eWLB package. Fig. 4 shows a RDL1 via for the TV-1. Fig. 5 illustrates four different RDL via structures for this study. Option 1 is a tapered via, which is used as a baseline case for the study. Other variations of via structures showed in Options 2, 3, and 4 are for a straight via, a combination of tapered vias and a thick Cu pillar, and a combination of tapered vias and a thin Cu pillar, respectively. The thermal loading condition of the FEA models were set to the temperature range from 250°C to -55°C and the stress free state at 150°C. The normalized maximum principal stress of BEOL layers with different via shape options and at different temperature conditions are compared in Table 3.

The BEOL layer has the lowest stress magnitudes with Option 2 while the highest stress magnitudes with Option 4, at temperature range of 125°C to -55°C. Generally, it is expected that thicker dielectric layers of low elastic moduli contribute to better decoupling effect between the RDL stack and BEOL layer at the temperature range of 125°C to -55°C. However, at the highest temperature of 250°C, it appears that the copper pillar structure serves as the reinforcement element to the Al pad to withstand the thermally induced stresses between the RDL stack and BEOL layer.

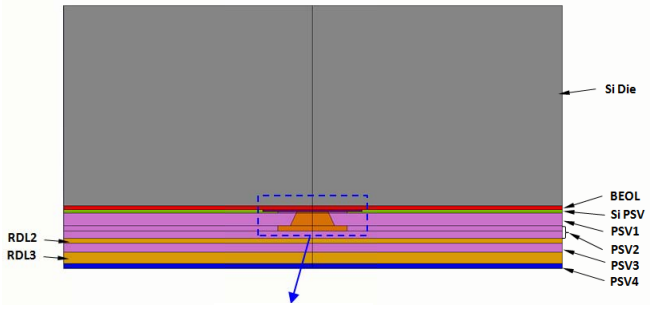
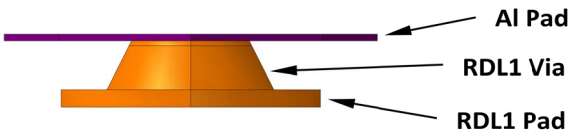
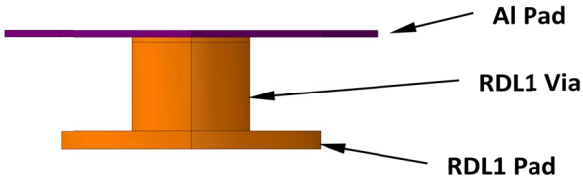


Figure 4. Schematic cross-section diagram of RDL1 via structure for TV-1.

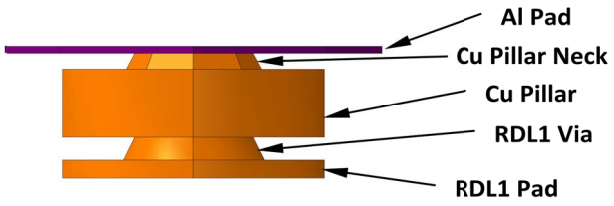
Option 1: Tapered Via



Option 2: Straight Via



Option 3: Via with Thick Cu Column



Option 4: Via with Thin Cu Column

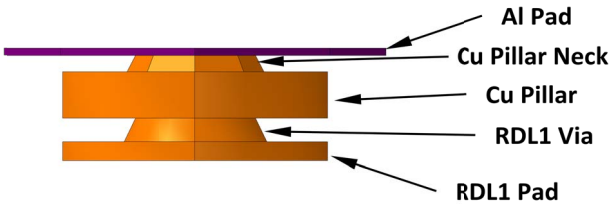


Figure 5. Design options of RDL via interconnection structures

Table 3. Normalized Max. Principal Stress.

Temperature (°C)	Design Option			
	1	2	3	4
250	1.00	0.91	0.87	0.79
125	1.00	0.93	1.15	1.20
25	1.00	0.88	1.04	1.09
-55	1.00	0.92	1.03	1.08

Thermal Characterization

For thermal characterization, the test vehicle was prepared with thermal die having thermal diode and heat block. Test vehicle specification was same as TV-2 in Table 2(b). The effect of die thickness effect was investigated with 3 different die thicknesses: 200um, 300um and 400um. For the comparison study, same die sizes for the flip chip package were prepared.

To easily detect the temperature at the hot spot of the die with applied power, all test vehicles had thermal die with a transistor and heating circuit block as well as temperature sensor. After surface mount technology (SMT) on a JEDEC standard 8-layer thermal test printed circuit board (PCB), 2.0W power was applied and junction temperature was measured with three different die thicknesses. As evident in Fig. 6, eWLB has a 10-15% improvement in thermal performance for the same die thickness as compared to flipchip packages. For eWLB, it can use a die that is thicker than flipchip package for embedding, achieving a more than 25% improvement in thermal performance with the same package height of eWLB compared to flipchip package.

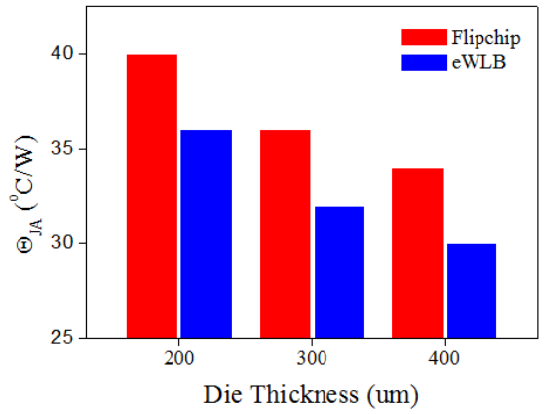


Figure 6. Experimental thermal characterization data of eWLB with different die thickness compared to flipchip.

Electrical Simulation& Characterization

Electrical Functional Characterization of eWLB[6]

Live dice from 28nm low power technology were assembled to make the electrical functional test vehicles. After assembling the eWLB test vehicles, final functional test, bench test and system level test (SLT), including test hardware of the flipchip, were performed with existing test infrastructure. The tests were carried out both at room temperature (25°C)and high temperature (110°C), and results show that test vehicles passed SLT testing and all stress tests (MSL3,TC, HTS) are supported by Table 2.
Test data shows eWLB performance is equivalent or slightly improved compared to flip chip with reduced metal layers from 6/4(in flip chip) to 3/2 (in eWLB) RDL layer. Multiple retests did not result in cracking and it proved the mechanical robustness of low profile eWLB package.

The CPI samples were functionally tested in Automated Test Equipment (ATE) with test handler. It passed most of test patterns and no failure was reported for package related[6]. Even for thinner body of eWLB did not have any issue of socket handling for test process. There was no obvious difficulty in handling on the ATE or socket, with no cracking of fragile die assembly.

Parasitic Electrical Simulation of eWLB and Flip Chip

The simulation modeling design was done with actual mobile product functional devices to find out package level performance in applications. In this design, a number of important pins were carefully selected and studied, such as the data, clock, VDD signal pins shown in Fig.7.

In this work, main findings are reported as below:

1. High-speed bus with each trace impedance-matched (e.g., to 50 Ohm)
2. Trace lengths are typically between 2 -3 mm
3. Trace distance to GND plane: 50 um for laminate, and 5 um for eWLB
4. eWLB is very thin package. As a result, the cross-talk in eWLB is typically much lower, more than 10 dB

Using computer simulation using commercial 2D electromagnetic field solver, the RLC parasitic values for eWLB and flipchip packages were found. Using ANSOFT HFSS software, the S-parameter of each of the packages were extracted. Table 4 illustrates the simulated results that were compared with RLC parasitic values and S parameters. For eWLB, it was reported as >60% reduction of inductance and resistance compared to flip chip and it was mainly due to its shorter interconnection length with thin film RDL without bump or organic substrate. It is also matched well with previous report of FOWLP parasitic work [7].

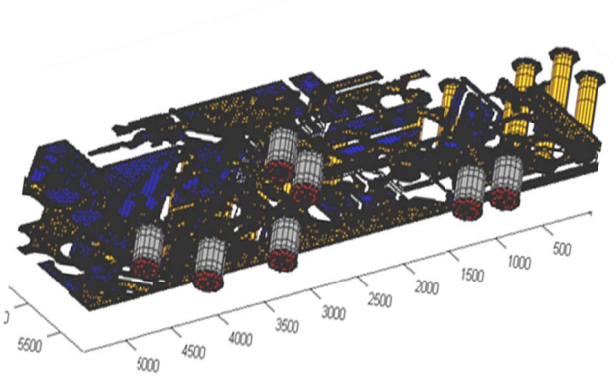


Figure 7. 3D electrical simulation modeling of eWLB.

Table 4. Comparison of electrical parasitic simulation result of eWLB and flipchip packages.

Net	Inductance, L (nH)			Resistance, R (mΩ)		
	flipchip	eWLB	Δ(%)	flipchip	eWLB	Δ(%)
1	1.77	0.43	-76%	240	67	-72%
2	2.03	0.24	-88%	308	42	-86%
3	1.51	0.57	-62%	348	112	-68%
4	1.08	0.25	-77%	268	66	-75%

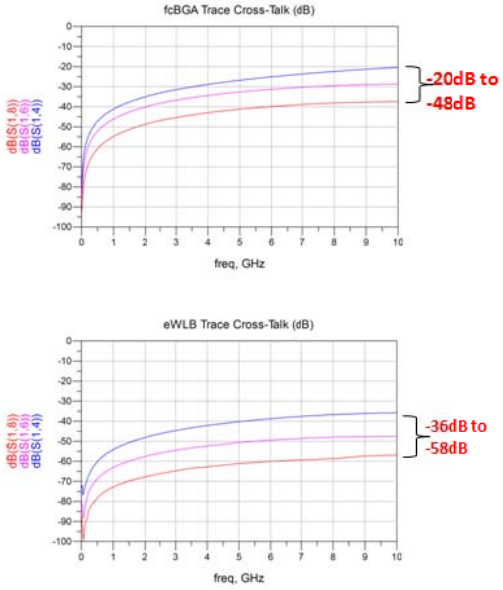


Figure 8 . Simulation of cross-talk for flipchip and eWLB.

III. CONCLUSION

Due to its materials and structure, eWLB technology is critical in wafer-level packaging solution that will help further develop and improve the emerging applications. In this study, 10x10~15x15mm 28nm eWLB CPI was researched and the paper reported on JEDEC standard component and board level reliability with various electrical, thermal and mechanical structural characterizations. The 28nm CPI test vehicles with advanced dielectric materials passed JEDEC reliability and they showed robust package reliability.

eWLB technology can promote heterogeneous integration between passives of inductors/resistor/capacitor into the various thin-film layers, active/passive devices into the mold compound or encapsulation, and to also achieve 3D vertical interconnections for new SiP as well as packaging solutions for 2.5D/3D. eWLB technology provides more holistic performance and has promising potential to be a new packaging solution that can widen its application range to plenty of types of automotive, 5G and mmWave applications, such as antenna on package (AoP) or antenna in package (AiP).

Acknowledgement

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