Board Level Reliability Improvement in eWLB (Embedded Wafer Level BGA) Packages

by

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ABSTRACT

When it comes to reducing form-factor and increasing functional integration of mobile devices, Wafer Level Packaging (WLP) is an attractive packaging solution with many advantages in comparison to standard Ball Grid Array (BGA) packages. With the advancement of various fan-out WLP (FOWLP), it is a more optimal and promising solution compared to fan-in WLP because it can offer greater flexibility in design of more Input/Output (I/O) counts, multi-chips, heterogeneous integration and three-dimensional (3D) system-in-package (SiP). embedded Wafer Level Ball Grid Array (eWLB) is a type of fan-out WLP enabling applications that require smaller form-factor, excellent heat dissipation, and a thin package profile as it has the potential to evolve in various configurations with proven manufacturing capacity and production yield. eWLB is one of key advanced packages because of advantages of higher I/O density, process flexibilities and integration capabilities. It facilitates integration of multiple dies vertically and horizontally in one package without using substrates. The structural design as well as selection of materials becomes more important in determining process yield and long term reliabilities. Therefore, it is necessary to comprehensively investigate the key design factors affecting the reliability.

In this paper, the influences of materials and structural designs on the board level reliability will be demonstrated. The structural analysis has been performed by going through every design factor in a board level. The reliability study was carried out in depth by experimental approaches as well as through thermo-mechanical simulations. The different structural design prolongs the life by giving more resistance to the crack propagation and also makes the entire package body more flexible. This paper also discusses the recent advancements of robust board reliability performance of large size eWLB. Standard JEDEC board level tests were carried out to investigate board level reliability of large size test vehicles and both destructive/non-destructive analyses were performed to investigate potential structural defects. Daisy chain test vehicles were also tested for board level reliability performance in industry standard test conditions.

I. Introduction

In just one decade the hand phone has transformed from a simple communication device into more complex system integrating features that allow customers to use it as a multipurpose gadget. The carrier technology has jumped from 1G to 3G, 3.5G, and LTE, changing at the rate of every two years and with room for potential growth with global adoption. Moving forward with this trend, packaging semiconductor devices for handheld electronics has become more challenging than ever before. Growing mismatch in interconnect gap, adding different functional chips for different features and application in similar system footprint and package size reduction to increase battery size for extended usage has opened the window for innovative embedding packaging technology.

New and emerging applications in the consumer and mobile space, the growing impact of the Internet of Things (IoT) and wearable electronics (WE), and the complexities in sustaining Moore's Law have been driving many new trends and innovations in advanced packaging technology. The semiconductor industry now has to focus on density scaling and system level integration to meet the ever-increasing electronic system demands for performance and functionality as well as the reduction of form factor, power consumption and cost.

This paradigm shift from chip scaling to system-level scaling has been reinventing microelectronics packaging, driving increased system bandwidth and performance, and helping to sustain Moore's Law. Demand for maximum functional integration in the smallest and thinnest package will continue to growth with an order-of-magnitude requirement for lower cost and power consumption. The challenge for the semiconductor industry is to develop a disruptive packaging technology capable of achieving these goals.

To meet the above said challenges, eWLB was developed which offers additional space for routing higher I/O chips on top of Silicon (Si) chip area which is not possible in conventional WLP or WLB [1]. It also offers comparatively better electrical, thermal and reliability performance at reduced cost with the possibility of addressing more Moore (decreasing technology nodes with low-k dielectrics in SoC) and more than Moore (heterogeneous integration of chips with different wafer technology as SiP solution in multi die or 3D eWLB approaches).

eWLB technology uses a combination of front- and back-end manufacturing techniques with parallel processing of all the chips on a wafer, which can greatly reduce manufacturing costs. Its benefits include a smaller package footprint compared to conventional leadframe or laminate packages, medium to high I/O count, maximum connection density, as well as desirable electrical and thermal performance. It also offers a high-performance, power-efficient solution for the wireless market [2].

eWLB (embedded Wafer Level BGA) Technology

eWLB technology is addressing a wide range of factors. At one end of the spectrum is the packaging cost along with testing costs. Alongside, there are physical constraints such as its footprint and height. Other parameters that were considered during the development phase included I/O density, a particular challenge for small chips with a high pin count; the need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency) [3].

The obvious solution to the challenges was some form of WLP. But two choices presented themselves: Fan-out or Fan-in. FO-WLP is an interconnection system processed directly on the wafer and compatible with motherboard technology pitch requirements. It

combines conventional front- and back-end manufacturing techniques, with parallel processing of all chips. There are three stages in the process. Additional fab steps create an interconnection system on each die, with a footprint smaller than the die. Solder balls are then applied and parallel testing is performed on the wafer. Finally, wafers are sawn into individual units, which are used directly on the motherboard without the need for interposers or underfill.

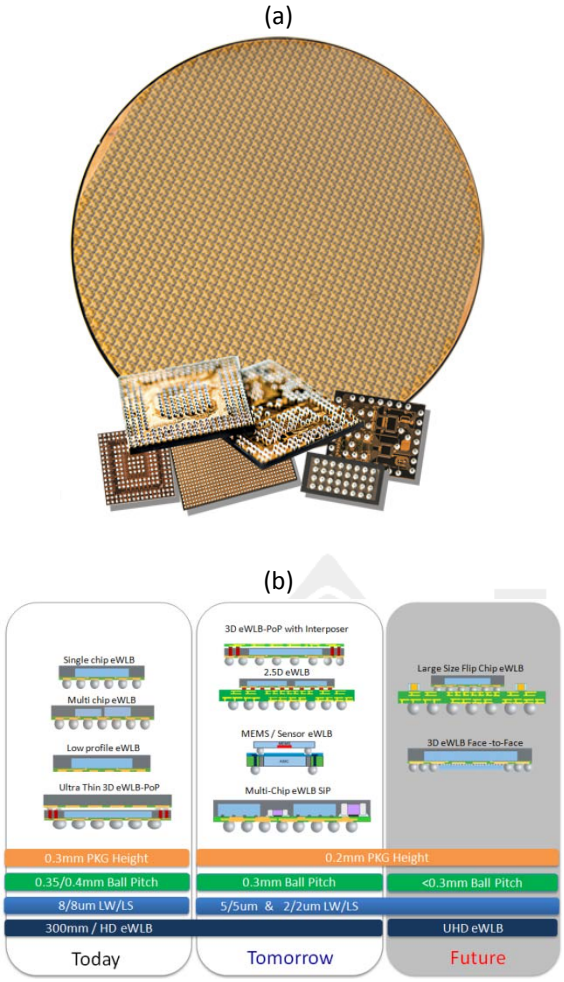

Figure 1. (a) 300mm eWLB carrier and eWLB packages, and (b) evolution of eWLB technology from 2D to 2.5D/3D packaging solution

The wafer level chip scale package (WLCSP) was introduced in the late 1990's as a semiconductor package wherein all manufacturing operations were done in wafer form with dielectrics, thin film metals and solder bumps directly on the surface of the die with no additional packaging [1]. The basic structure of the WLCSP has an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides and back of the die. The WLCSP is the smallest possible package size since the final package is no larger than the required circuit area. Although WLCSP is now a widely accepted package option, the initial acceptance was limited due to concerns with the Surface Mount Technology (SMT) assembly process and the fragile nature of the exposed silicon inherent in the package design. Assembly skills and methods have improved since the introduction of WLCSP, however, damage to the exposed silicon remains a concern. This is particularly true for advanced node products with fragile dielectric layers.

A new process has been developed to provide five-sided protection for the exposed silicon in a WLCSP, therefore achieving a true known-good WLCSP. The ability to apply a protective coating to all the exposed die surfaces in a WLCSP with encapsulation, RDL, and bumping "burn-in" process is based on an existing high volume manufacturing flow developed for fan-out products known as embedded Wafer Level Ball Grid Array (eWLB). Unlike conventional WLP, the first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Although this is commonly done for other semiconductor package formats, it has not been practiced for conventional WLP. Following singulation, the diced silicon wafers are then reconstituted into a standardized wafer (or panel) shape for the subsequent process steps. [2].

II. Modeling and Experimental Results

In this study, 3D full package finite element analysis (FEA) models were constructed due to the asymmetric nature in package structure, e.g. ball layout and die position. Table 1 shows the test vehicle package specification. Test vehicles were mounted on a 1.00mm thick printed circuit board (PCB) in accordance to JEDEC Specification JESD22-B111. For a light weight package, it was found that collapsed solder bump shape after reflow can be reasonably estimated using truncated-sphere theory as reported in [4]. All models were subject to the temperature cycling condition ranged from -40 to 125°C, with 10 minutes ramp and 5 minutes dwell times. Except for solder balls, all materials were assumed to be linear elastic as shown in Table 2. Anand constitutive model [5] was used to represent the inelastic deformation behavior of the lead-free solders. Three nodes at the test board bottom surface were chosen to be fixed with Ux=Uz=0, Ux=Uy=Uz=0, and Uz=0 to prevent the rigid body movement. Solder fatigue life model can be generally expressed through a power law relationship as the following form:

$$N_f = \alpha(\Psi)^{-\beta}$$

where N_f is the number of cycles to failure, Ψ is a damage parameter, α and β are empirical fitting parameters determined by least-squares regression analysis. In this study, characteristic life (63.2% of unreliability rate) is used as the solder fatigue life.
Equivalent creep strain or creep strain energy density accumulated per stable cycle can be chosen as the damage parameter for evaluating the solder joint fatigue life.Critical solder joint can be identified by the maximum value of the chosen damage parameter.

Table 1. Test Vehicle Package Specification

Item	Description
Package Type	eWLB
Package size	6 x 6 mm
Die Size	4.5 x 4.0 mm
Bump Count	150
Bump diameter/pitch	0.250/0.400 mm
Bump Material	SAC305

Table 2. Material properties of eWLB package assembly

Constituent	Young's Modulus (MPa)	Poisson's Ratio	Tg (°C)	CTE1 / CTE2 (ppm/°C)
Die	131000	0.28	-	2.7
Molding Compound	22000	0.30	160	7.4 / 33
Dielectric Layer	2500	0.33	210	54
BSP Tape	6800	0.33	59	71 / 115
Metal Pad	118000	0.35	-	17.3
PCB	22000	0.39	140	16.6
Solder (SAC305)	41600	0.35	-	21.7

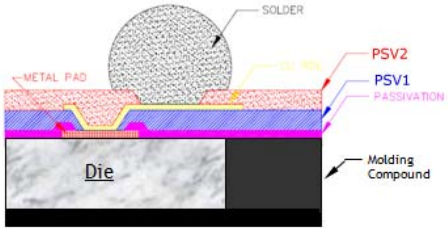

Figure 2 . Cross-section Diagram of eWLB with 1L-RDL

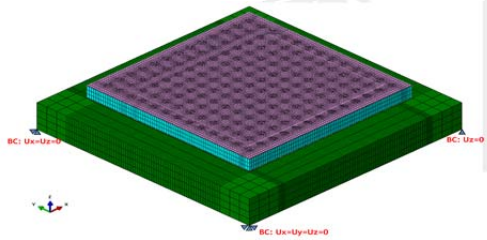

Figure 3. FEA Model of eWLB Package

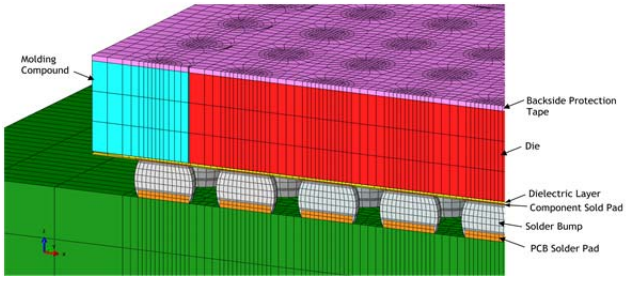

Figure 4. Internal Cutout View of eWLB Package

A. Package Thickness

For studying of TCoB performance as a function of package thickness, simulation study was carried out for 3 different package thicknesses, i.e., 0.45, 0.33 and 0.25mm.

Figure 5 shows the creep strain plot shows that the critical failure location is near the top side of corner solder bump.

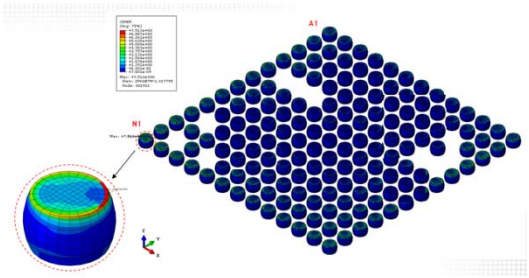

Figure 5. Creep Strain Distribution Plot for Solder Joints of 475um Thick eWLB at End of Third Cycle

As shown in below Table 3, TCoB performance improves with thinner package. Also experimental daisy chain test data shows good agreement of improved reliability with thinner package as shown in Figure 6.

Table 3. Effect of package thickness on TCoB reliability.

Leg	Pkg Thk (mm)	Predicted $N_{63.2\%}$ (Normalized)	Change (%)
1	0.475	100	Baseline
2	0.330	120	+20%
3	0.250	131	+31%

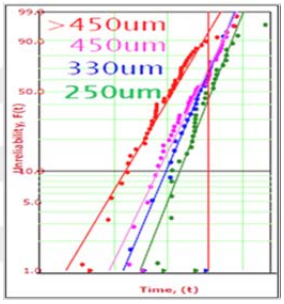

Figure 6. Weibull Plot of Daisychain TV of TCoB Reliability Tests.

B. Die position

Die position is also critical to board level reliability performance in eWLB FOWLP for effective CTE of package. In this study we have two simulations of die-centered and off-centred designs as shown in Figure 7. Table 6 shows that there is less TCoB performance off-centred eWLB compared to die-centred structure. It is therefore critical to put die in center or nearby centre to keep good TCoB performance. Once die is moved to corner or off-centered area, then effective DNP was increased and local effective package CTE is also increased so it would provide lower TCoB performance.

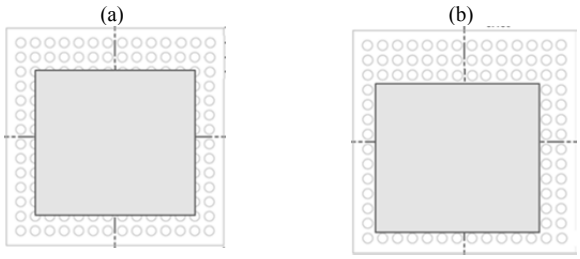

Figure 7. Die position in eWLB (a) Centred and (b) Off-centred

Table 3. Effect of die position on TCoB reliability

Leg #	Die Position	Predicted $N_{63.2\%}$ (Normalized)	Change (%)
1	Centre	100	Baseline
2	Off-Centre	89	-11%

C. Corner Ball Connection

Corner ball is considered as the most weakest point due to its larger DNP (Distance from Neutral Point), thus receiving the highest stress in most cases. It is quite critical for board level reliability of wafer level packaging so it is highly recommended to remove corner ball connection. A 20-30% improvement was reported with no corner-ball connection in conventional WLCSP. Below Table 3 shows the similar findings.

Table 3. Effect of corner ball connection on TCoB reliability

Leg #	Corner Ball Connection	Predicted $N_{63.2\%}$ (Normalized)	Change (%)
1	Connected	100	Baseline
2	Not Connected (NC)	121	+21%

D. Solder Mask Opening Size

Solder mask opening size effect is studied for TCoB performance with same size solder ball. There are two case studies of 475 and 250um package thickness. With a larger solder mask opening size, TCoB performance is improved and it is more effective with thinner package height. As shown in Table 4. Larger solder mask opening provides larger solder bonding area (+18%) so it may accommodate more energy to propagate crack in larger area.

Table 4. Effect of solder mask opening size on TCoB reliability

Leg #	PKG Thickness	Solder Mask Opening Size (um)	Predicted $N_{63.2\%}$ (Normalized)	Change (%)
1	475	240	100	Baseline
2	475	260	126	+26%
3	250	240	131	+31%
4	250	260	156	+56%

E. Solder ball pitch and solder ball size

In order to study solder ball pitch and solder ball size effect on TCoB, below 3 different DOEs were prepared and simulated. Simulation data shows larger solder pitch would have less reliable TCoB performance due to its overall lower number of IOs.

Table 5. Effect of solder ball pitch and ball size on TCoB reliability

Leg #	SolderBall pitch (um)	Solder Ball Size (um)	Predicted $N_{63.2\%}$ (Normalized)	Change (%)
1	400	250	100	Baseline
2	500	300	95	-5%
3	650	300	53	-47%

III. Summary and Conclusions

For eWLB FOWLP, various design factors were studied and evaluated for improved TCoB.

1. Thinner package has significant improvement of TCoB reliability
2. Die position is critical and it would be preferred to locate in die centre area to get better TCoB reliability.
3. No connected corner ball is effective to improve TCoB reliability.
4. Larger Solder mask opening size significantly improve TCoB reliability.

Among various design factors in this study, their impacts on eWLB TCoB performance can be generally ranked in descending order as below

PKG thickness > no-corner ball connection > larger solder mask opening > Die position.

For further improvement of TCoB performance of large eWLB FOWLP, package design and structure optimization is important and there would be several combined effect using above mentioned considerations.

eWLB technology is an important wafer-level packaging solution that will enable the next-generation of a mobile, IoT and wearable applications. The advantages of standard fan-in WLPs, such as low assembly cost, minimum dimensions and height, as well as excellent electrical and thermal performance, are equally true for eWLB. The differentiating factors with eWLB are the ability to integrate passives like inductors, resistors and capacitors into the various thin-film layers, active/passive devices into the mold compound, and achieve 3D vertical interconnections for new SiP and 2.5D/3D packaging solutions. Next-generation eWLB technology will play an important role in the new wave of mobile, IoT and wearable devices today, and in the near future.

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