

Panel Level Advanced Packaging

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**Originally published in the 2016 IEEE 66th Electronic Components and Technology Conference
Proceedings, Las Vegas, Nevada, May 31 – June 1, 2016.
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Abstract—Advanced packaging technology is the catalyst that enables greater chip connectivity needed for the never-ending quest for more powerful mobile devices, tablets, Internet of Things (IoT) and wearable devices with increased functionality that operate with lower power requirements for extended battery life but remain available at low cost. The evolution of advanced packaging to incorporate 2.5D and 3D processes into production space puts additional pressure upon outsourced assembly and test (OSAT) facilities and foundries to maintain costs and production efficiencies and accentuates the opportunity to move from manufacturing advanced packaging on circular wafers to rectangular substrates e.g. panel level advanced packaging. Migrating from circular wafers to rectangular substrates provides OSATs with the means to process more die per substrate to increase productivity and yield while reducing manufacturing costs.

This paper demonstrates panel level advanced packaging on rectangular substrates is practicable. Lithographic results for resolution and overlay imaged on rectangular substrates populated with test die will be presented. Specific requirements and challenges encountered for successful registration between layers are discussed, along with solutions that were implemented to meet the design goals. Challenges that remain will also be highlighted.

Panel level advanced packaging throughput advantages will also be reviewed. Throughput achieved on rectangular substrates will be presented and compared to throughput for similar devices on circular wafers. Throughput will be analyzed to demonstrate why throughput on a rectangular substrates is advantageous over circular wafers with review of panel level advanced packaging enabling the population of whole die in the corners of the panel without the loss of partial die experienced on the radius of a circular substrate. Reduction in nonproductive overhead to manufacturing equipment when panel level advanced packaging is adopted will also be presented.

Keywords—Advanced packaging, panel level advanced packaging, OSAT, 2.5D, 3D, TSV, overlay, throughput

I. INTRODUCTION

The evolution of semiconductor packages is driven by consumer demand for mobile phones, tablets, IoT and wearable devices. Advanced packaging has enabled integration of devices with new capabilities to meet the need for increased functionality that consumers demand. Manufacturing has evolved from wafer level chip scale packaging (WLCS) to fan out wafer level processing (FOWLP) and 2.5 and 3D processing. Evolution of the innovative technology employed to fabricate devices with increased functionality at affordable costs requires OSATs and foundries to employ emerging manufacturing technologies that reduce costs while increasing output. Migrating to panel-based processing will increase the number of die processed per substrate and will result in significant productivity improvement over conventional wafer-based processing that has been employed to date (Fig. 1). The toolset that has been developed by the semiconductor industry and used for the production of flat panel displays, PCB and solar panels provides the ability to migrate from wafer based processing to panel based processing. [1]

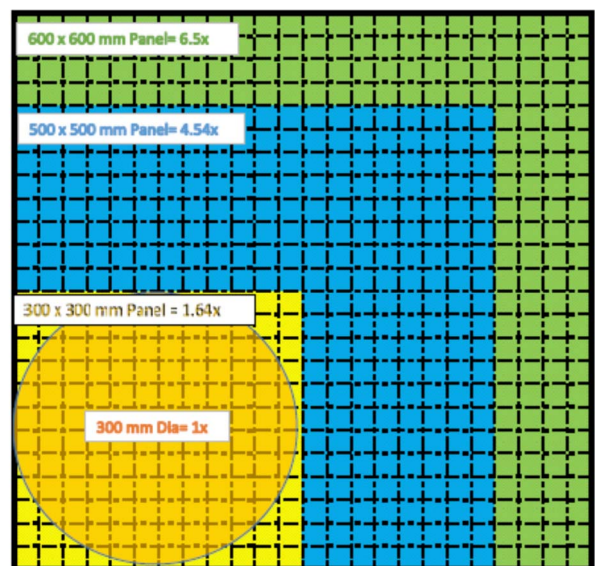


Figure 1. Comparison of number of die exposed on 300 mm wafer to number of die on panel.

A. Panel-based Lithography Requirements

Lithography remains a key requirement for advanced packaging on panels. The same lithography requirements of resolution, overlay and yield that apply to wafer processing will also apply to panel processing. Since panels have a larger exposure area than wafers the lithography system should have the capability to expose a larger exposure field size per exposure while maintaining imaging and overlay characteristics that are required for the process. Exposing a larger field size per exposure reduces the number of exposures required per panel, resulting in higher throughput. Larger exposure field size also provides a means to avoid stitching of fields as fan out sizes become larger.

To expose a larger field size and maintain overlay from layer to layer the lithography system also needs the capability to correct for scale and magnification across the larger image field as well as compensate for die placement inaccuracy realized with reconstituted panels by the gantry used to populate the panel or curing of the mold compound. A single telecentric lens system with adjustable reticle positioning for magnification, trapezoid in x and y, rotation, and xy translation is appropriate to achieve overlay with the larger exposure field. This capability enables corrections for intra field magnification, scale, theta and compliments corrections made by the xy stage for orthogonality, theta and scale.

Die placement on reconstituted panels for fan out are sensitive to the same constraints experienced with reconstituted wafers. Die placement accuracy by the gantry used for pick and place as well as the molding process contribute to die offsets on the substrates that must be understood by the lithography stepper to achieve targeted overlay. Another feature that is also beneficial, if utilized, is “mapping” of a panel to measure the actual die placement position in relation to its designed location and providing this information to the stepper for the best possible alignment solution to achieve overlay at different areas of the panel. Mapping of die location was first practiced in the 1980s on lithography steppers used in front-end applications. In practice, not every layer needs to be mapped because alignment keys for subsequent layers are imaged during the first exposure layer and they become the alignment targets for remaining layers. An example of a mapped panel is shown in Fig. 2.

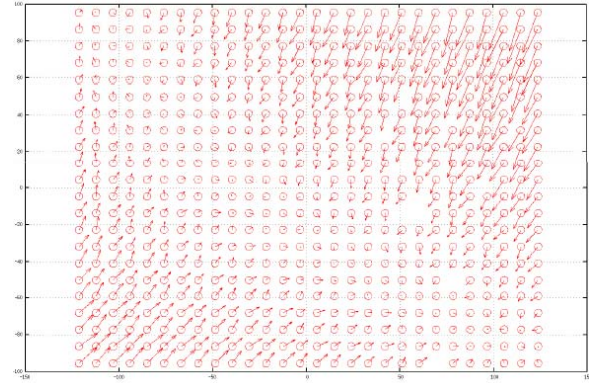


Figure 2. Vector map of die placement offset on a reconstituted panel illustrating various die shift across the panel. Circle radius is 4 μm .

B. Large Area Exposure Field

A large area exposure field is desirable to minimize the number of exposures per substrate and realize throughput benefits. To validate use of a larger exposure field a test was developed that imaged a field size of 59.4 x 59.4 mm on a substrate with pre-designed die placement offsets. Results in Fig. 3 show that max overlay offset of 15 μm was achieved on exposure of substrates with >40 μm of pre-designed die placement offset. This level of overlay was achieved by using the local alignment system of the stepper to measure actual die placement position of specific areas of the substrate and automatically adjusting the stepper's magnification and grid scale to expose the 59.4 x 59.4 mm exposure area and achieve overlay across the entire exposure field.

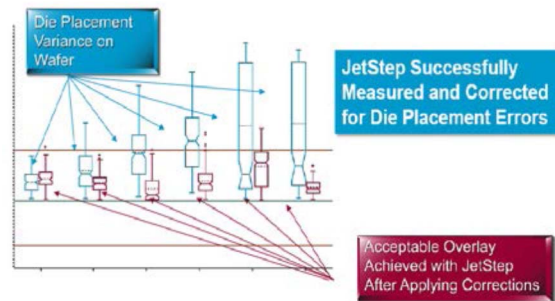


Figure 3. Box plot showing overlay achieved with large exposure field on substrates with pre-designed die placement offsets.

C. Overlay Achieved with Applied Alignment Strategy

Numerous panels have been processed to investigate the adoption of panel-based advanced packaging. The panels were exposed on a Rudolph Technologies JetStep® lithography system. The JetStep system is a 2x reduction lithography stepper with a single telecentric optical system that exposes a 59.4 x 59.4 mm exposure area (84 mm dia.) on the

panel while enabling magnification adjustment on a per panel basis along with grid corrections for scale. Magnification and scale can be corrected for up to ± 400 ppm or $\pm 16.495 \mu\text{m}$ of correction from center to diagonal edge of exposure field (Fig. 4). Distortion is tightly controlled within $<0.1 \mu\text{m}$ of distortion over the magnification and scale adjustment range. [2]

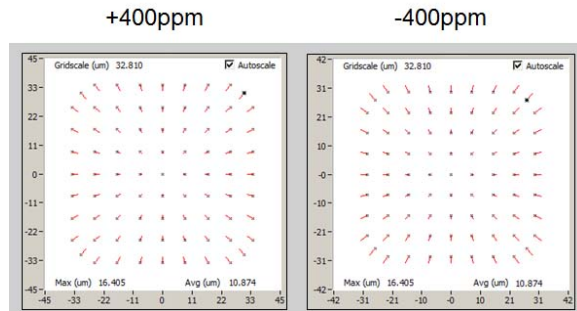


Figure 4. Vector map showing available magnification and scale adjustment over an 84 mm diameter lens field.

Each panel was mapped before exposure to determine the actual die position relative to its designed location. The mapped data was then analyzed by an on board stepper utility and an exposure array generated with corrections applied from the mapped data for magnification, scale, orth and rotation.

An example of mapped data and expected results are shown in Fig. 5 below.

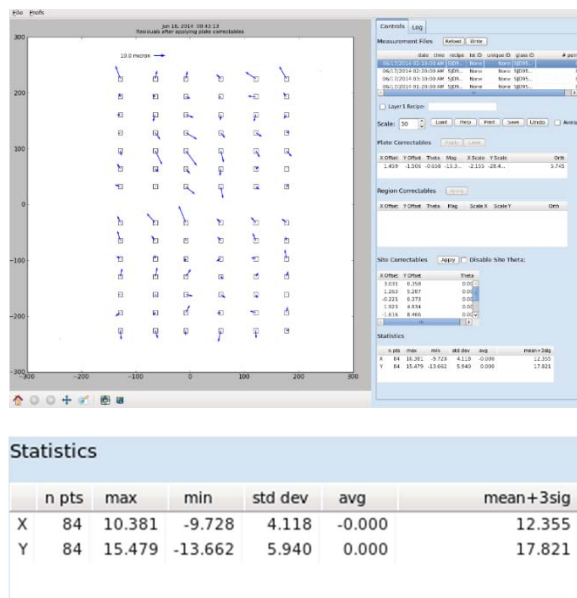


Figure 5. Vector map of die offset across panel.

Visual inspection of the panel after exposure resulted in vias centered on the pad across the panel. (Fig. 6, 7).

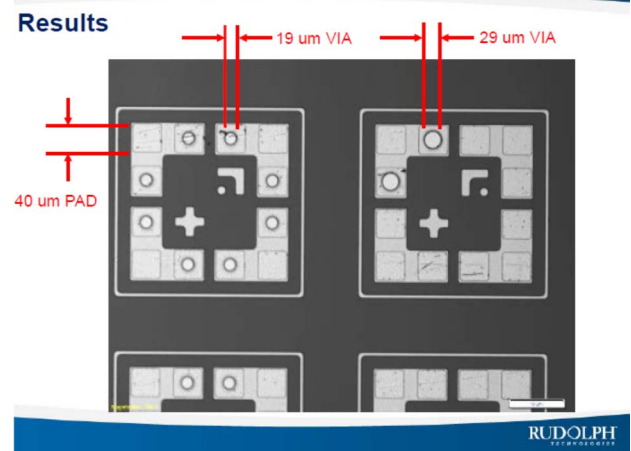


Figure 6. Via to pad overlay on panel test structure.

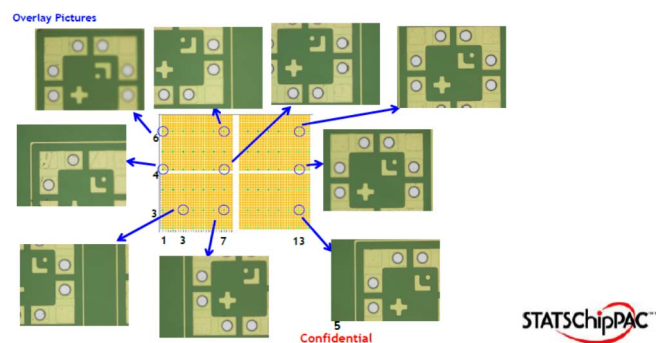


Figure 7. Test panel showing acceptable overlay across panel.
Source: STATS ChipPAC

D. Resolution and Depth of Focus

Advanced packaging requires resolution of features in thicker films than used in front-end applications. Additionally, die-to-die and within die topographical variation occurs due to embedding and bumping process. Resolution is not sub-micron but aspect ratios of up to 6:1 can be expected and require optical systems with adequate numerical aperture (n.a.) to achieve desired resolution while imaging through the thick film and across the topography. Advanced packaging benefits from steppers utilizing optical systems with lower n.a. to increase depth of focus (DOF) and image through the thick films and over the topography required for advanced packaging applications. Achievable resolution and DOF are determined by the following equations;

$$R = k_1 \lambda / n.a.$$

$$DOF = k_2 \lambda / n.a.^2$$

Where k_1 and k_2 are process factors, λ is wavelength.

If DOF is not sufficient, patterning and process latitude in thick film stacks will be limited. Features and aspect ratios that may be exposed for advanced packaging are shown. Large DOF is required to achieve imaging such as this (Figs. 8, 9, 10). [3]

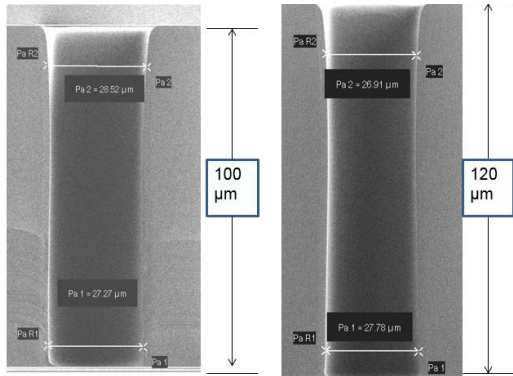


Figure 8. 28 μm via imaged in 100 and 120 μm thick film thickness for 4:1 aspect ratio.

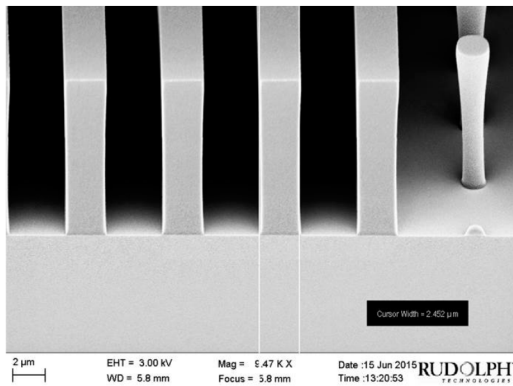


Figure 9. 3 μm redistribution layer (RDL), 11.5 μm FT, 3.8:1 aspect ratio in TOK photoresist

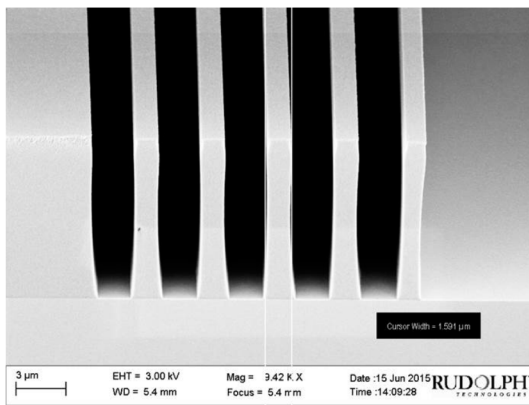


Figure 10. 2 μm RDL, 11.5 μm FT, 5.75:1 aspect ratio in TOK photoresist.

E. Resolution Patterning on Panels

Accurate dose control and focus is required across the panel to achieve the desired resolution at all locations on the panel. Panels have larger area than wafers and determining focus at each exposure location requires the ability to individually focus at each exposure site on the panel.

To evaluate resolution performance across panels, focus exposure arrays were exposed at nine locations across the panel and resolution and DOF evaluated (Fig

11). The panels were coated by either slit coating technology or spin coated and developed with the appropriate developer for the material being evaluated. A sample of resolution achieved is shown in Fig. 12.

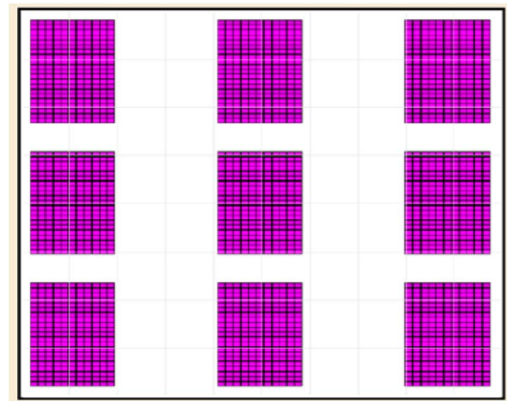


Figure 11. Focus exposure matrix imaged at nine locations across the panel.

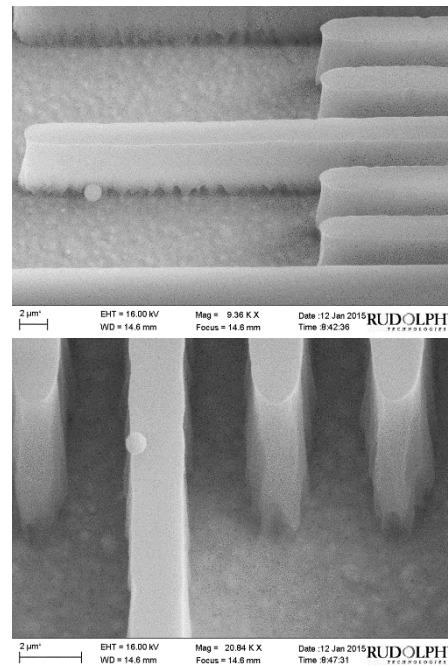


Figure 12. Copper clad panel. 2 μm resolution. 10 μm film thickness. Sumitomo photoresist.

F. Warpage

Warpage is recognized as an issue with 300 mm reconstituted wafers. The stepper and handling equipment must accommodate for warpage that is incurred due to the molding operation or various films that are deposited on the substrate. Panel warpage is also an area that will need to be addressed. Some of the handling characteristics currently employed in reconstituted wafer processing can be employed to handle panels, but panels also have unique characteristics that are different than wafers because

they are rectangular in shape and flex and distort differently than a wafer. Steppers currently utilized for the manufacture of flat panels are experienced with handling large glass substrates of up to 920 x 730 mm at 0.3 mm thickness that flex considerably during handling. This technology can be utilized to successfully transfer and vacuum panels used for advanced packaging to the stage chuck.

G. Panel Throughput Advantage

Manufacturing costs are a concern in any industry. For advanced packaging lithography the opportunity to move from circular wafers to rectangular substrates provides a means to reduce manufacturing costs by utilizing tool sets that have been developed for the production of flat panel displays, printed circuit boards and solar panels. All use manufacturing processes that can be applied to advanced packaging on large rectangular substrates.

Front-end lithography is performed on round wafers and die are lost at the edge of the wafer due to portions of the square die laying beyond the radius of the wafer e.g. “square peg in round hole”. As discussed above, exposure fields for advanced packaging are large and can expose multiple die with each exposure. Since a wafer is populated to contain all known good die (KGD) within the exclusion area of the wafer the advantage of exposing multiple die in a large single exposure is compromised along the wafer edge because only a portion of the die are exposed, due to the way a wafer is populated, and the remaining exposure area is nonproductive because it lays in the wafer exclusion zone or off the edge of the wafer. It stands to reason that exposing a square or rectangular pattern fits more perfectly on a square or rectangular substrate and eliminates lost opportunity that occurs on wafers because a portion of the exposure area lies beyond the edge of a circular wafer (Fig. 13). Larger rectangular substrates also increase throughput by reducing nonproductive overhead required to exchange substrates.

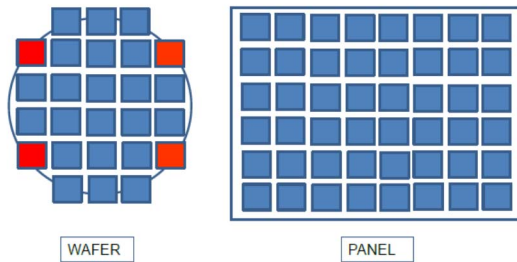


Figure 13. Illustration of partial die exposure on a wafer compared to die exposure on a panel. Exposures with non-productive area are shown in red.

Productivity gains from exposing panels instead of wafers has been modeled by comparing exposure of various die sizes (Table I and Fig. 14) on a 600 x 600

mm² panel to the same die size on 300 mm diameter wafers. Processing conditions are 1500kW/cm² at ghi wavelength with nine alignment sites per substrate and substrate transfer constant at 14 seconds.

Results show a productivity increase of >96% in the number of die realized per hour on the panel process over the wafer process.

TABLE I.

Die size (mm ²)	Panel		Wafer		% Productivity increase per hour of panel over wafer
	Die per 600 x 600 mm ² panel	Die per hour	Die per 300 mm wafer	Die per hour	
4.05 x 2.6	28,350	643.5k	5,945	328k	96
2.44 x 2.44	51,750	1174k	10,442	556k	111
4.95 x 5.4	10,800	246k	2,339	123k	100

Die size (mm ²)	Exposure Field at Substrate (mm ²)	Exposures per Substrate		Substrates per Hour	
		Wafer 300 mm	Panel 600 x 600 mm ²	Wafers	Panel
4.05 x 2.6	61.87 x 56.200	25	100	55.3	21.7
2.44 x 2.44	62.885 x 57.848	27	100	53.3	20.9
4.95 x 5.4	60.28 x 54.720	28	90	52.5	22.8

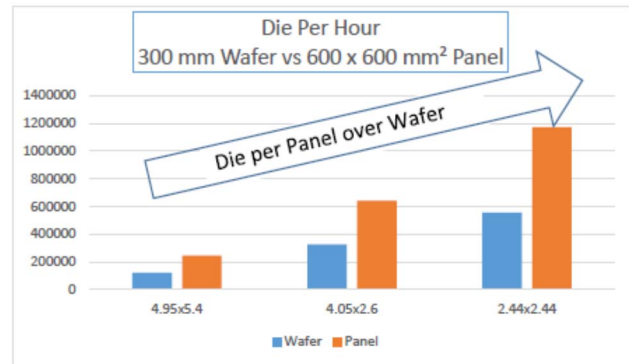


Figure 14. Productivity increase that can be expected when processing on 600 x 600 mm² panel over 300 mm diameter wafer.

The tables above demonstrate the productivity advantage of exposing on rectangular substrates versus circular wafers. In panel processing, the number of exposures per panel increases due to the larger area of the panel and processed panels per hour are less then processed wafers per hour. However, the number of die populated on a panel is much greater than the number of die populated on a wafer, resulting in a >96% productivity advantage when exposing on panels instead of wafers.

H. Panel Inspection

The advanced packaging market is also continuously pushing for smaller line space and line width redistribution layers (RDL) on these fan-out packages. This drives the need for high resolution inspection that is capable of handling and inspecting large panels. Also as discussed earlier, the warpage on the panels presents significant challenges to not only handling but also detection of sub-micron defects. To inspect these warped panels, Rudolph Technologies Firefly™ S Inspection System maintains focus by rapidly moving the imaging objective and slowly moving the optical head to maintain sharp imagery throughout the inspection. The system is capable of compensating for die placement accuracy of each die independently in real time as it maintain focus while the panel is scanned.

In addition, substrates may be organic and even on epoxy molded compound (EMC) approach, there are organic material related defects that are very hard to detect using standard bright-field or dark-field illumination. The system is equipped with a fluorescent image based high speed detection that is capable of finding these organic residue defects which are largely undetected today. Typically RDL defects of interest are half the size of the RDL width e.g. 1 μ m for 2 μ m RDL. But in many cases, the acceptable metal graininess could be larger than the detection size. This leads to a high nuisance rate impacting the total throughput of the panel which includes manual review. The fluorescent technique resolves this issue as the metal does not fluoresce and hence the metal grains are not detected as defects while finding 1 μ m open or short in the RDL lines.

For cost effective deployment, the system is also integrated with a metrology sensor capable of simultaneous thickness measurements of transparent material and RDL height metrology. The inspection and metrology data is exported to Rudolph's Discover® software system to analyze electrical, metrology and defect data in a single source. This enables faster root cause analysis enabling quicker ramp and time to market.

II. CONCLUSION

Migrating from circular substrates to square or rectangular panels provides OSATS with the means to increase productivity per substrate processed. The improved fit between the mask and substrate on square or rectangular substrates, instead of circular wafers, during exposure eliminates nonproductive exposure of partial die about the periphery of a circular substrate and enables more die per substrate to be exposed. Exposing on panels provides a cost effective lithographic solution to an OSAT or foundry with a >96% productivity improvement over wafer-based processing.

The semiconductor industry has been a leader in adopting manufacturing technologies to fabricate devices with increased functionality while reducing manufacturing costs. This has enabled consumer acceptance and adoption of new technologies that are in demand throughout the world. Silicon wafers have increased in diameter from 4, 6, and 8 inches to 300 mm and eventually 450 mm. Imaging square die on circular wafers will result in nonproductive exposures around the diameter because a square peg does not fit efficiently into a round hole. Implementing panel-based processing is not evolutionary, instead, it is the natural progression to achieve greater throughput at a cost advantage.

ACKNOWLEDGMENT

The authors wish to thank STATS ChipPAC for the panels they provided and continued support through this project. The authors also thank Keith Best, Jack Mack, Jim Webb and several Rudolph personnel around the world that have contributed to collecting data included in this paper.

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