Advanced 3D eWLB PoP (embedded Wafer Level Ball Grid Array – Package on Package) Technology

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ABSTRACT

The advancement of silicon scaling to 14/16 nanometer (nm) in support of higher performance, higher bandwidth and lower power consumption in portable and mobile devices is pushing the boundaries of emerging packaging technologies to smaller fan-out packaging designs with finer line/spacing as well as improved electrical performance and passive embedded technology capabilities. Advanced embedded Wafer Level Ball Grid Array (eWLB) technology provides a versatile platform for the semiconductor industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D System-in-Package (SiP) configurations.

The industry adoption of PoP as a dominant packaging approach in stacking the logic processor and memory into a single solution for advanced mobile phones and tablets has accelerated the need to drive ultra thin package profiles in this technology. Earlier in 2012, eWLB-PoP technology delivered a 30% height reduction in PoP, reducing the overall stacked package height from the industry standard 1.4mm to 1.0mm. Through further innovations in eWLB technology, a 40% height reduction in the bottom PoP architecture has been acheived. An ultra thin z-height of 0.3mm was realized in 2013, thereby providing the advantage of having an overall PoP package height as low as 0.8mm with proven board level reliability. While traditional PoP solutions are widely used in the high-end mobility market, demand is accelerating for ultra thin, cost effective packages that have the flexibility to serve a range of applications from mid-range to low-end mobile phones as well as tablets that require significantly higher processor speeds. While PCB substrate technology limits the interconnection density of a PoP package to 200-300 I/O, eWLB-based PoP solutions can deliver beyond 500 I/O in an overall thinner package with a dense vertical interconnection and wider interface to stack memory packages on the top.

This paper reports developments that extend 3D PoP applications with eWLB technology, including ultra thin or/and with an interposer substrate attachment. Various test vehicles have been designed and fabricated to demonstrate these low profile solutions for mobile, portable and wearable electronics. The test vehicles have ranged from medium to large sizes up to ~225mm2 and 0.4mm ball pitch. Mechanical, thermal and electrical characterizations are to be discussed with component and board level reliability results. Innovative structure optimization that provides dual advantages of both height reduction and enhanced package reliability are reported. To enable higher interconnection density and signal routing, packages with multi layer redistribution (RDL) and fine line/width spacing are fabricated and implemented on the eWLB platform. Successful reliability characterization results on 3D eWLB-PoP package configurations are reported as an enabling technology for highly integrated, miniaturized, low profile and cost-effective 3D packaging solutions.

I. Introduction

In just one decade hand phone has transformed from a simple communication device into more complex system integrating features that allow customers to use it as a multipurpose gadget. The carrier technology has jumped from 1G to 3G,3.5G, LTE changing at the rate of every two years and with room for potential growth with global adoption. Moving forward with this trend, packaging semiconductor devices for handheld electronics has become more challenging than ever before. Growing mismatch in interconnect gap, adding different functional chips for different features and application in similar system footprint and package size reduction to increase battery size for extended usage has opened the window for innovative embedding packaging technology.

New and emerging applications in the consumer and mobile space, the growing impact of the Internet of Things (IoT) and wearable electronics (WE), and the complexities in sustaining Moore's Law have been driving many new trends and innovations in advanced packaging technology. The semiconductor industry now has to focus on density scaling and system level integration to meet the ever-increasing electronic system demands for performance and functionality as well as the reduction of form factor, power consumption and cost.

This paradigm shift from chip scaling to system-level scaling is and will continue to reinvent microelectronics packaging, drive increased system bandwidth and performance, and help sustain Moore's Law. Demand for maximum functional integration in the smallest and thinnest package will continue to growth with an order-of-magnitude requirement for lower cost and power consumption. The challenge for the semiconductor industry is to develop a disruptive packaging technology capable of achieving these goals.

To meet the above said challenges eWLB was developed which offers additional space for routing higher I/O chips on top of Silicon chip area which is not possible in conventional WLP or WLB[1]. It also offers comparatively better electrical, thermal and reliability performance at reduced cost with possibility to address more Moore (decreasing technology nodes with low-k dielectrics in SoC) and more than Moore (heterogeneous integration of chips with different wafer technology as SiP solution in multi die or 3D eWLB approaches).

eWLB technology uses a combination of front- and back-end manufacturing techniques with parallel processing of all the chips on a wafer, which can greatly reduce manufacturing costs. Its benefits include a smaller package footprint compared to conventional leadframe or laminate packages, medium to high I/O count, maximum connection density, as well as desirable electrical and thermal performance. It also offers a high-performance, power-efficient solution for the wireless market[2].

eWLB (embedded Wafer Level BGA) Technology

eWLB technology is addressing a wide range of factors. At one end of the spectrum is the packaging cost along with testing costs. Alongside, there are physical constraints such as its footprint and height. Other parameters that were considered during the development phase included I/O density, a particular challenge for

small chips with a high pin count; the need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency) [3].
The obvious solution to the challenges was some form of WLP. But two choices presented themselves: Fan-out or Fan-in. FO-WLP is an interconnection system processed directly on the wafer and compatible with motherboard technology pitch requirements. It combines conventional front- and back-end manufacturing techniques, with parallel processing of all chips. There are three stages in the process. Additional fab steps create an interconnection system on each die, with a footprint smaller than the die. Solder balls are then applied and parallel testing is performed on the wafer. Finally, wafers are sawn into individual units, which are used directly on the motherboard without the need for interposers or underfill.

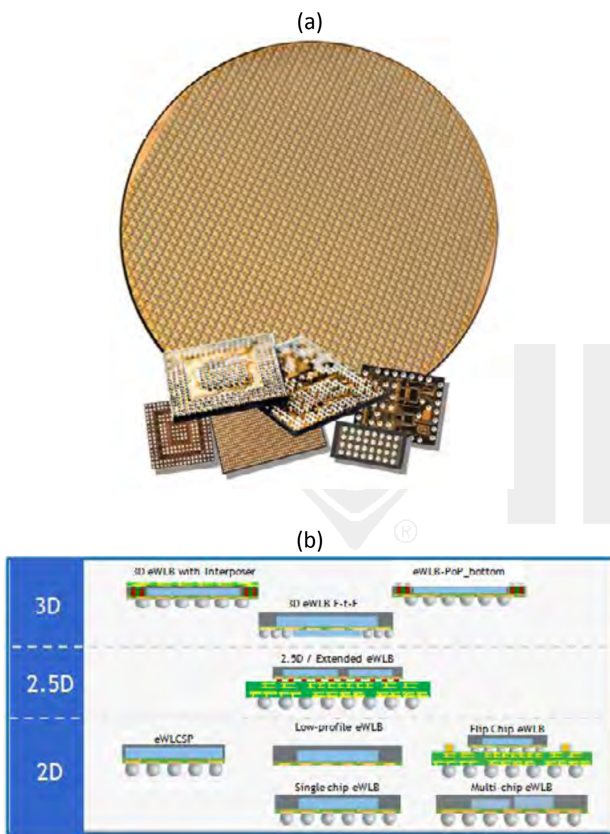

Figure 1. (a) 300mm eWLB carrier and eWLB packages, and (b) evolution of eWLB technology from 2D to 2.5D/3D packaging solution

The wafer level chip scale package (WLCSP) was introduced in the late 1990's as a semiconductor package wherein all manufacturing operations were done in wafer form with dielectrics, thin film metals and solder bumps directly on the surface of the die with no additional packaging [1]. The basic structure of the WLCSP has an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides and back of the die. The WLCSP is the smallest possible package size since the final package is no larger than the required circuit area. Although WLCSP is now a widely accepted package option, the initial acceptance was limited due to concerns with the Surface Mount Technology (SMT) assembly process and the fragile nature of the exposed silicon inherent in the package design. Assembly skills and methods have improved since the introduction of WLCSP, however, damage to the exposed silicon remains a concern. This is particularly true for advanced node products with fragile dielectric layers.

A new process has been developed to provide five-sided protection for the exposed silicon in a WLCSP, therefore achieving a true known-good WLCSP. The ability to apply a protective coating to all the exposed die surfaces in a WLCSP with encapsulation, RDL, and bumping "burn-in" process is based on an existing high volume manufacturing flow developed for fan-out products known as embedded Wafer Level Ball Grid Array (eWLB). Unlike conventional WLP, the first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Although this is commonly done for other semiconductor package formats, it has not been practiced for conventional WLP. Following singulation, the diced silicon wafers are then reconstituted into a standardized wafer (or panel) shape for the subsequent process steps as shown in Figure 1.

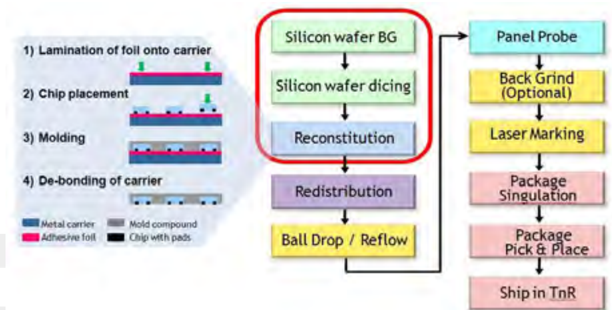

Figure 1. eWLB Process Flow

The reconstitution process as shown on the left in Figure 1 includes four main steps.

1) The reconstitution process starts by laminating an adhesive foil onto a carrier.

2) The singulated die are accurately placed face down onto the carrier with a pick and place tool.

3) A compression molding process is used to encapsulate the die with molding compound while the active face of the die is protected.

4) After curing the molding compound, the carrier and foil are removed with a de-bonding process, resulting in a reconstituted wafer where the molding compound surrounds all exposed silicon die surfaces.

The eWLB process is unique in that the reconstituted wafer does not require a carrier during the subsequent wafer level packaging processes. The implementation of this process flow into 300mm diameter reconstituted wafers has been described in detail in previous presentations [2].

FlexLine™ : Breakthrough Manufacturing Method for Wafer Level Packaging

A new manufacturing method, FlexLine™, has been developed to produce a wafer level package that severs the link between wafer diameter and wafer level packaging methods[4]. The new manufacturing method is wafer size agnostic, so one manufacturing module can produce fan-in, fan-out, and 3D fan-out products

regardless of the incoming wafer size. The same bill of materials, manufacturing methods and manufacturing location can produce wafer level packages from any size silicon wafer. Since the manufacturing module is wafer size agnostic, there is no risk of capital for investment in the manufacturing infrastructure. A change in loading between 200mm, 300mm, and 450mm wafers does not adversely affect the utilization of the manufacturing module. The process also enables new advanced wafer level packages otherwise unattainable with conventional manufacturing methods. FlexLine™ seamlessly processes multiple silicon wafer diameters on the same manufacturing line and produces both fan-out and fan-in devices as illustrated in Figure 2. FlexLine™ provides the ability to scale a device to larger panel sizes for a compelling cost reduction compared to conventional wafer level packaging methods. The FlexLine™ process has been qualified at advanced silicon nodes down to 22nm, ball pitches down to 0.40mm and body sizes as small as 2.5x2.5mm.

Figure 2: FlexLine™ seamlessly processes multiple silicon wafer diameters on the same manufacturing line to produce both FIWLP and FOWLP.

3D eWLB-PoP Technology

The continued demand for higher level of integration has led to the industry's adoption of 3D packaging technologies and, in particular, the Package-On-Package (PoP) configurations. This technology allows for vertical integration of the memory package and the logic package into one stacked package. The top package is primarily a memory module including some combination of Flash and SDRAM, while the bottom package typically contains the logic die, which is a baseband or an application processor of some kind. Top and bottom package are connected via the pads that are located on the top side of the bottom PoP package, and these pads are used to connect the top PoP (memory module) Ball Grid Array (BGA) solder balls to the bottom PoP package. There are various PoP package types including bare-die PoP, Embedded Solder On Pad (eSOP) PoP, and Laser-Via PoP that have proliferated to meet the increasing market demand[5].

(a)

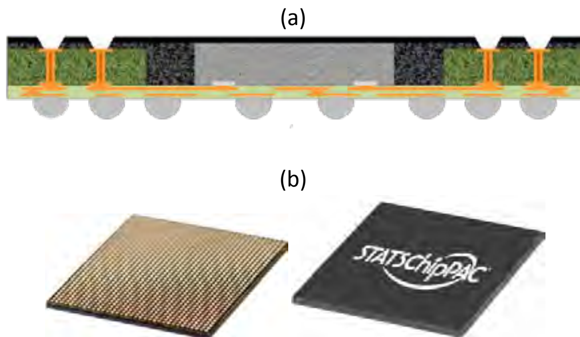

Figure 2. (a) Schematics of package structure of 3D eWLB-PoP bottom and (b) 3D eWLB-PoP stacked (with top memory package) of total 0.8mm height.

3D eWLB-PoP has unique advantage due to adoption of merits of each two technologies so it bring significant advantages in profile and cost compared to current PoP technologies. 3D eWLB-PoP is designed to meet the lower profile PoP requirement for mobile or tablet application with cost-effective solution. 3D eWLB-PoP bottom has 300um package height so total eWLB-MLP could be less than 0.8 mm after top package stacking (body thickness of 0.45mm) Table 1 shows value proposition of 3D eWLB-PoP technology.

Table 1. Value proposition of eWLB-PoP

1. *PoP packages larger than 15x15mm have been enabled using eWLB HVM processes*
2. *Ultra Thin PoP solutions of 0.8mm total stacked package (300um total bottom package thickness with embedded high density vias).*
3. *Package successfully passed all Component Level and Board Level Reliability Tests*
4. *Enhanced thermal and electrical performance with shorter interconnection length compared to flipchip or WB solutions*
5. *Well controlled warpage for thinner package height*
6. *Top ball pitch comes down to 0.2mm (~ 1000 I/O in 14x14mm PKG)*
7. *Pre-stacked assembly option available for top package*

II. Experimental Results

Test Vehicle Specification

For further process development and reliability tests, two test vehicles were designed as shown in Table 2. Both packages are used for further component/board level reliability tests with ball shear and OS (open-shot) tests. For TV2, this specification is to used for thermal characterization with thermal die assembly. Also functional devices of TV1 and TV2 are assembled for electrical functional characterization compared to fcPoP.

Table 2. eWLB-PoP Test vehicles specification

	TV1	TV2
Package body size	10x10mm	15x15mm
die size	50mm^2	110mm^2
Top ball pitch	0.4mm	0.4mm
Bottom ball pitch	0.4mm	0.4mm
Ball size	0.25mm	0.25mm
Body thickness	0.2mm	0.25mm

(a) (b)

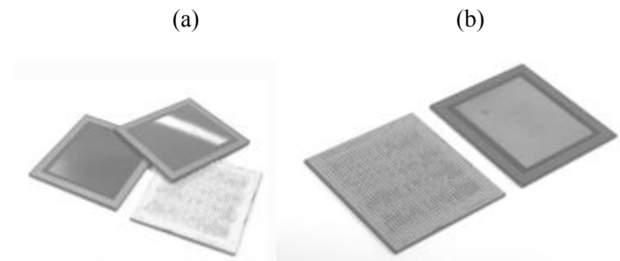

Figure 3. Micrograph of 3D eWLB-PoP; (a) TV1 and (b) TV2

Component Level Reliability
Table 3 shows the package level reliability result of each next generation 3D eWLB packages. They passed JEDEC (Joint Electron Device Engineering Council) standard package reliability test such as MSL (Moisture Sensitivity Level) 3 with Pb-free solder conditions. Test vehicle (TV1/2) has 10x10mm 3D eWLB-PoP. It successfully passed all industry standard package level reliability with ball shear test and OS(open-short) test.

Table 3. Package Level Reliability Results of 3D eWLB-PoP.

Reliability Test	JEDEC	Test Condition	Read-out	Results
Unbiased HAST (W/ MSL3)	JESD22-A118	130°C, 85%RH	168hrs	Pass
Temperature Cycling (TC-B, w/MSL3)	JESD22-A104	-55°C/125°C; 2Cy/hr	1000x	Pass
High Temp. Storage (HTS)	JESD22-A103	150°C	1000hr	Pass

Board Level Reliability
For board level reliability tests, eWLB-PoP (stacked with top package) was assembled and mounted on PCB. For PoP assembly, 450um height eWLB (body thickness is 250um) top packages were assemble and total eWLB-MLP stacked package shows 750-800um height. Those samples were tested in JEDEC TCoB and drop reliability test conditions.
Table 4 shows 3D eWLB-PoP board level reliability of JEDEC TCoB and Drop test results of test vehicle 1 and 2 (Table 2 and Figure 3). Test vehicles were PoP stacked with top memory package. There was TCoB first failure after 1000 cycles. Drop reliability performance was robust and showed no failure after 300 drops. These test results show the robustness of board level reliability of 3D eWLB-PoP.

Table 4. Board Level Reliability Test Results of 3D eWLB-PoP

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103 -40°C to 125°C	Pass
Drop Test	JEDEC JESD22-B111 1500G	Pass

Experimental Thermal Characterization of 3D eWLB-PoP

For thermal characterization, test vehicle was prepared with thermal die. Test vehicle specification is same as TV2 in Table 2(b). dy, die thickness effect was studied with 200um, 300um and 400um body thickness. Also same size of fcPoP were prepared for comparison study.

All test vehicles have thermal die with transistor and heating block as well as temperature sensor so it easily detects temperature at hot spot of die. After SMT on thermal test board, 2.0W power was applied and measured junction temperature with various die thickness. As shown eWLB-PoP has 8-10% thermal performance improved for same die thickness as compared to fcPoP. For eWLB, it can use thicker die than fcPoP for its embedding, >20% improvement of thermal performance with same PKG height of eWLB-PoP compared to fcPoP.

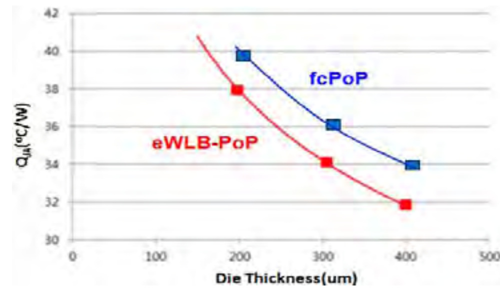

Figure 4. Thermal characterization data of 3D eWLB-PoP with different die thickness compared to fcPoP.

Electrical Functional Characterization of 3D eWLB-PoP
Functional devices of TV1 and TV2 were assembled with 28nm low power technology. After assembly of 3D eWLB PoP, final functional test, bench test and system level test (SLT) were performed with existing test infrastructure included test hardware of fcPoP. Test was also carried out at room temperature and hot-test of at 110C. SLT testing was performed and passed including stress tests (MSL3,TC, HTS) as shown in Table 3.
Test data shows 3D eWLB-PoP performance is equivalent or slightly improved compared to fcPoP solutions. Multiple retest does not result in cracking and it proved mechanical robustness of low profile 3D eWLB-PoP.

3D eWLB-PoP for SiP solutions
FO-WLP in a 3D configuration has received considerable customer interest for memory and advanced application processors by virtue of the higher routing density and form factor reduction. The requirement for SiP integration is also a growing trend for advanced application processors, MEMS and sensors in wearable electronics as way to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor[6].

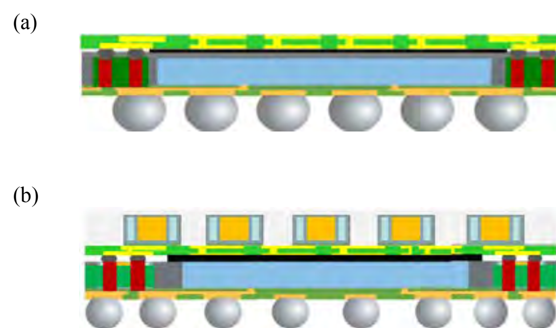

Figure 5. Schematics of SiP eWLB-PoP: (a) with interposer and (b) discretes on interposer or top package of discretes.

Figure 5 shows one of example of SiP eWLB-PoP which that has a number of discretes in the top package and is pre-stacked on the bottom eWLB to form a 3D SiP module with a thin profile. Discretes are removed from the motherboard and relocated in the top package

for a reduction in the space required on the mother board. Discretes are also more effective when they are close to the device, which significantly improves the overall performance as well as provides a power saving advantage. This SiP eWLB-PoP has demonstrated more attractive power efficiency performance compared to conventional packaging and it is representative of a significantly smaller packaging solution that is well-suited for IoT or WE devices.

III. Conclusions

Rapid growth of emerging mobile, IoT and WE devices will be enabled only by more compact and low-cost semiconductor packages with increased performance and packaging complexity. Wafer-level technology effectively accommodates new lithography nodes and provides a strong packaging platform to address performance, form factor, integration and cost requirements. In addition to providing higher bandwidth, ultra high-density, embedded capabilities, and improved thermal dissipation in a small, thin package format, advanced wafer-level packaging is an alternative for small flip-chip and large QFN packages and is quickly becoming a package of choice in the evolving mobile, IoT and WE markets. Fan-out wafer-level technology also provides the ability to tightly manage the co-design process and achieve silicon optimization, which is increasingly important in ultra cost-sensitive markets.

Advanced packaging plays a crucial role in delivering achieving higher performance, lower power, lower cost, and a smaller form factor. There are many challenges that have been, and are being resolved in the application of cost-effective materials and processes for various reliability and security requirements for new and emerging mobile, IoT and WE applications. The industry requires innovation in packaging technology and a cost-effective high-volume manufacturing process that is able to meet current and forecasted market demands.

eWLB technology is an important wafer-level packaging solution that will enable the next-generation of a mobile, IoT and wearable applications. The advantages of standard fan-in WLPs, such as low assembly cost, minimum dimensions and height, as well as excellent electrical and thermal performance, are equally true for eWLB. The differentiating factors with eWLB are the ability to integrate passives like inductors, resistors and capacitors into the various thin-film layers, active/passive devices into the mold compound, and achieve 3D vertical interconnections for new SiP and 2.5D/3D packaging solutions. Next-generation eWLB technology will play an important role in the new wave of mobile, IoT and wearable devices today, and in the near future.

Advanced low profile 3D eWLB-PoP was developed using eWLB (FO-WLP) technology. It passed JEDEC standard component level reliability conditions. PoP, package stacking and board level reliability were carried out and showed robust reliability in TCoB and drop tests. Thermal and functional electrical characterization were carried out and it showed its enhance performance compared to fcPoP.

3D eWLB-PoP / SiP eWLB-PoP technology provides more value-add in performance and promises to be a new packaging platform that can expand its application range to various types of mobile/portable devices as well as 3D SiP systems.

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