Ultra Fine Pitch RDL Development in Multi-layer eWLB (embedded Wafer Level BGA) Packages

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Abstract

The market for portable and mobile data access devices connected to a virtual cloud access point is exploding and driving increased functional convergence as well as increased packaging complexity and sophistication. This is creating unprecedented demand for higher input/output (I/O) density, higher bandwidths and low power consumption in smaller package sizes. There are exciting interconnect technologies in wafer level packaging such as eWLB (embedded Wafer Level Ball Grid Array), 2.5D interposers, thin PoP (Package-on-Package) and TSV (Through Silicon Via) interposer solutions to meet these needs.

eWLB technologies with the ability to extend the package size beyond the area of the chip are leading the way to the next level of high density, thin packaging capability. eWLB provides a robust packaging platform supporting very dense interconnection and routing of multiple die in very reliable, low profile, low warpage 2.5D and 3D solutions. The use of these embedded eWLB packages in a side-by-side configuration to replace a stacked package configuration is critical to enable a more cost effective mobile market capability. Combining the analog or memory device with digital logic device in a semiconductor package can provide an optimum solution for achieving the best performance in thin, multiple-die integration aimed at very high performance.

This paper highlights the rapidly moving trend towards eWLB packaging technologies with ultra fine 2/2μm line width and line spacing and multi-layer RDL. A package design study, process development and optimization, and mechanical characterization will be discussed as well as test vehicle preparation. JEDEC component level reliability test results will also be presented.

Key words

eWLB, Fanout wafer level package, fine line width and space, multi-layer RDl, reliability

I. Introduction

As a small, lightweight, high performance semiconductor package, wafer level chip scale packaging (WLCSP) has been a popular solution for space constrained mobile devices and is a compelling solution for new IoT and WE applications. WLCSP was introduced in the late 1990's as a semiconductor package wherein all manufacturing operations are performed in wafer form with dielectrics, thin film metals and solder bumps applied directly on the surface of the die with no additional packaging [2]. The WLCSP provides the smallest possible package size since the final package is no larger than the die itself. The volume of WLCSP packages used in the industry has experienced steady growth since its introduction -- driven by the small form factor and high performance requirements of mobile consumer products [1].

For emerging applications requiring significantly higher performance and bandwidth, a transition from fan-in WLCSP to fan-out wafer level packaging (FOWLP) is required to achieve maximum connection density, improved electrical and thermal performance and small package dimensions. FOWLP, also known as embedded Wafer Level Ball Grid Array (eWLB), is an interconnection system processed directly on the wafer and is compatible with motherboard technology pitch requirements

eWLB technology addresses a wide range of factors for mobile, IoT and WE applications. At one end of the spectrum is the need for a significant increase in input/output (I/O) density, a particular challenge as packages become progressively smaller and thinner. eWLB technology delivers fine line width and spacing as well as superior electrical performance, providing more design flexibility and a more significant reduction in size than is possible with printed circuit board (PCB) substrate technology. Along with this there is the need to integrate different active and passive elements, embedded very close to each other as a system-in-package (SiP). There complex thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency) are successfully addressed by eWLB technology[2]. On the other side of the spectrum is the need to reduce assembly and test costs to meet consumer market requirements. The manufacturing process for eWLB is well established and lends itself to the use of large wafer and panel sizes, which has a direct impact on capital intensity and cost.

eWLB for mobile applications

As demonstrated by the evolution of cellular phones, product differentiation today is driven by ever-expanding functionality, feature sets, and faster communications. At the same time, consumers have made clear their desires for feature-rich products in compact form factors to enable maximum portability. eWLB technology is enabling semiconductor manufacturers to provide the smallest possible and the highest performing semiconductors. Currently eWLB devices are used in baseband processors, RF transceivers, connectivity, near field communication (NFC), security devices, microcontrollers (MCU), memory, memory controllers, RF-MEMS and power management ICs. There has been a steady customer adoption and added opportunities such as MEMS, fingerprint sensors and wearable electronics. eWLB devices are found in all leading mobile products as well as in consumer electronics.

At present, the primary high volume ICs are baseband, RF Transceiver, power management integrated circuits (PMIC), NAND memory controller, connectivity, and security devices. Accelerated near-term customer adoption is taking place in logic processors, RF, audio and connectivity devices, 77GHz ADAS automotive devices, and MEMS/sensor devices. eWLB solutions are now in high volume production on 28 nm Si node and starting to ramp 20 nm devices.

In a number of cases, eWLB achieved a 20~40% reduction in package size as compared to other packaging solutions and over 50% volume reduction due to its slim and smaller form factor. For RF and high frequency devices, eWLB showed less parasitic electrical performance thus it also significantly improved overall device performance. In one example, a 77 GHz SiGe mixer packaged as an eWLB achieved excellent high frequency electrical performance due to the small contact dimensions and short signal pathways which decreased parasitic effects. A higher power efficiency was found in eWLB solutions for PMIC devices compared to other package solutions.

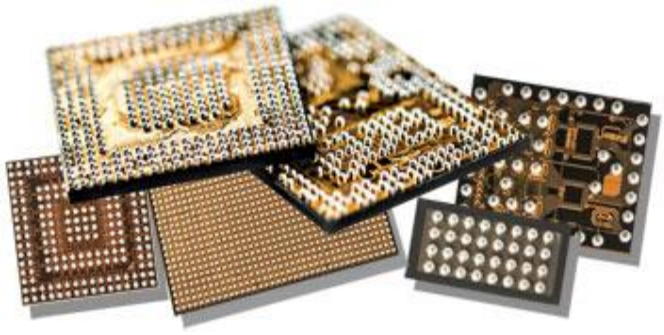


Fig. 1 eWLB products found in various mobile products and consumer electronics

II. Fine Line Width and Spacing with multi-layer RDL structure in eWLB

In situations where a device may have an interconnect pad arrangement or wafer level component, an additional layer of lateral connections may be employed to rearrange the connections in a manner suitable for wafer level processing. This additional layer is known as a redistribution layer or RDL and fabricated from a thin layer of metal with dielectrics in between. RDL is for higher electrical performance and complex routing to meet electrical requirements.

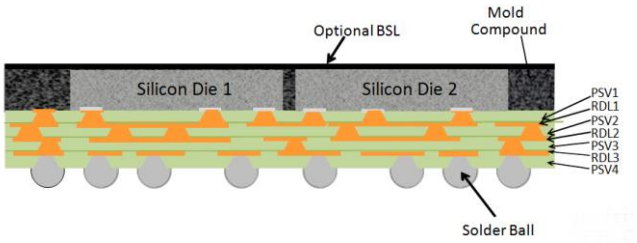
In FOWLP/WLCSP designs, the I/O pads are placed in uneven distributions, so we need a ReDistribution Layer (RDL) to connect these pads to the ball. From package to board, a similar redistribution is also needed for the signal array to escape outward to other devices. A test vehicle was designed per technical specification of Table 1. It has 3-layer RDL structure with 2/2, 5/5, 10/10um line

width/spacing in multi-die eWLB structure. Fig. 2 shows the schematics of 3-layer RDL process flow for test vehicle preparation. Table 2 shows the each layer thickness of 3-L RDL eWLB test vehicle. 3-layer RDL was prepared by the process flow shown in Fig. 3 with current HVM process equipments in eWLB/FlexLine™.

Table 1. Technical specification of test vehicle.

Die Size	Die1: 11.0 x 6.0 mm Die2: 11.0 x 6.0 mm
PKG Size	15x15mm
Ball Pitch	400um
Die Thickness	200um
Package ball height/size	185um
PKG Thickness	400um

(a)



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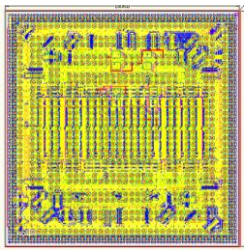

Fig. 2 (a) Schematics of cross-section and (b) 3-layer RDL design layout of test vehicle

Table 2. RDL stackup layer thickness of test vehicle of Fig.2

Each Layer	**Thickness**
RDL1	3um
RDL2	4um
RDL3	8um

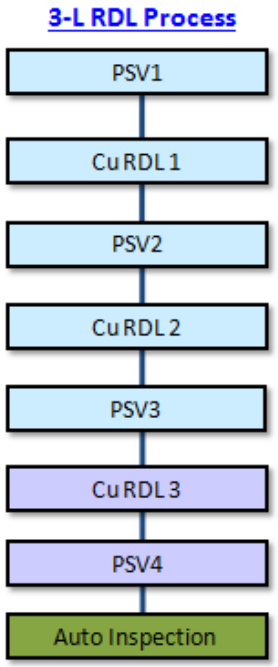

Fig.3 3-layer RDL process flow

A. 2/2um and 5/5um Line Width and Spacing RDL

One of the greatest challenges facing wafer level packaging at present is the availability of routing and interconnecting high I/O fine pitch area array. RDL (redistribution layer) allows signal and supply I/O's to be redistributed to a footprint larger than the chip footprint in eWLB. Required line widths and spacing of 2/2 µm for eWLB applications support the bump pitch of less than 40um. Finer line width and spacing are critical for further design flexibility as well as electrical performance improvement. For die-to-die interconnects of high I/O or multi channels, finer line is critical for multi-die design and routing flexibility.

Figs. 4 - 6 show 5/5um and 2/2um LW/LS RDL, respectively as per RDL process flow of Fig.3. Micrographs show uniform and well defined micro structure. Cu RDL thickness and CD are also well controlled. Even with mixed design of finer and coarse LW/LS. With this process development, it is verified of robust process of fine RDL fabrication using current HVM equipments and process flow.

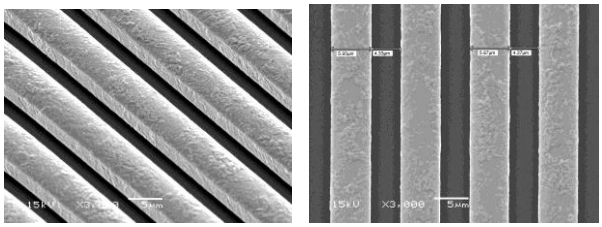

Fig. 4 SEM micrograph of 5/5um LW/LS RDL.

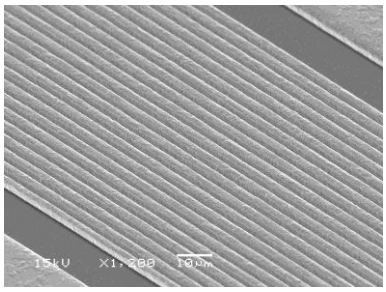

Fig. 5 SEM micrograph of 2/2um LW/LS RDL.

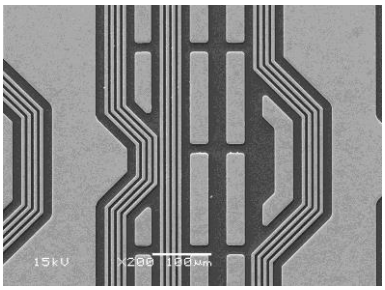

Fig. 6 SEM micrograph of mixed LW/LS design RDL structure.

B. 3-layer RDL with fine LW/LS.

Side-by-side multichip packaging can provide more design flexibility for SiP applications because a chip designer has more freedom in pad location as well as circuit block allocation. eWLB technology utilizes very fine pitch metal line width and space as well as multi-layer RDL process, so it provides better technical solutions for multi-chip packaging. eWLB uses fine pitch metallization and well controlled interconnection with wafer fab lithography process thus it has great advantage to provide better electrical performance compared to conventional flipchip technology. Fig.7 shows the cross-section of 3-layer RDL test vehicle with its CD measurements.

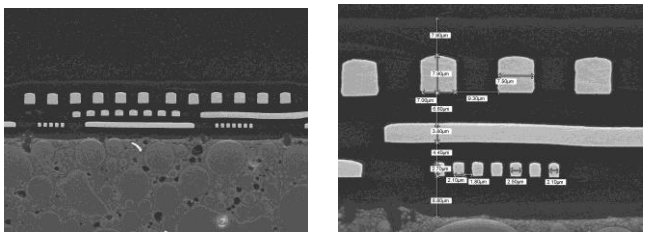

Fig. 7 SEM micrograph of 3-layer RDL eWLB

III. Reliability Test Results

A. Leakage Current Test

Leakage current test is to measure the undesirable leakage current that flows through or across the surface of the insulation or the dielectric of a capacitor. This test is generally carried out at 2 volt of the rated input voltage of the samples under test. This test is used to help ensure that the processes and assembly practices are satisfactory and reliable.

For 2/2um and 5/5um LW/LS test vehicle, leakage current was measured as shown in Table 3. It shows quite robust leakage current performance for both ultra fine LW/LS.

Table 3 Leakage current test results of 2/2um and 5/5um LW/LS TV.

TV #1	2/2um (pA)	5/5um (pA)	TV#2	2/2um (pA)	5/5um (pA)
AVG	1.271	1.397	AVG	1.047	1.164
MAX	3.066	3.143	MAX	1.750	2.543
MIN	0.437	0.481	MIN	0.149	0.224

B. Component Level Test

JEDEC Standard reliability tests of test vehicles with 3-layer RDL and 2/2um LW/LS were completed as shown in Table 1 and Fig.2. It passed JEDEC standard reliability tests used in wafer level packaging. Component level reliability was completed with the test conditions shown in Table 4.

Table 4. Component Level Reliability Results

Component Level Test	Condition		Status
MSL1	MSL1, 260°C Reflow (3x)	-	Pass
Temperature Cycling (TC) after Precon	-55°C to 125°C	1000 x	Pass
HAST (w/o bias) after Precon	130°C / 85% RH	192 hrs	Pass
High Temperature Storage (HTS)	150°C	1000 hrs	Pass

IV. Conclusion

In this study, ultra fine 2/2um LW/LS with 3-layer RDL was demonstrated and characterized in eWLB technology. It also passed JEDEC component level reliability test results. It provides high density interconnection such as die-to-die connects or high IO applications, such as graphics, network or high performance devices. It would be critical factor for next gen wafer level paging including 2.5D/3D integration

Advanced packaging plays a crucial role in driving products with increased performance, low power, lower cost and smaller form factor. There are many challenges that have been and are being resolved in the application of cost effective materials and processes for various reliability and security requirements. The industry requires innovation in packaging technology and manufacturing to meet current and forecasted demands and the ability to operate equipment in high volume with large throughput.

eWLB technology is an important complementary solution to standard WLPs, enabling the next generation of a mobile, IoT and wearable applications.. The benefits of standard fan-in WLPs such as low packaging/assembly cost, minimum dimensions and height as well as excellent electrical and thermal performance are equally true for eWLB as well. The ability to integrate passives like inductors, resistors and capacitors into the various thin film layers, active/passive devices into the mold compound and 3D vertical interconnection opens additional design possibilities for new Systems-in-Package (SiP) and 2.5D/3D packaging. Moreover, next generation, SiP-eWLB/3D eWLB technology provides more value-add in performance and promises to be the new packaging platform that can expand eWLB application range to various types of devices for true 3D SiP/module systems.

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