WLCSP+ and eWLCSP in FlexLine: Innovative Wafer Level Package Manufacturing

by

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Abstract

The demand for Wafer Level Chip Scale Packages (WLCSP) has experienced tremendous growth due to the surge in demand for advanced mobile products. The increased demand is seen for both 200mm wafers and 300mm wafers, however a significant segment of the market continues to be driven by 200mm designs. The infrastructure capacity supporting 200mm WLCSP has been stressed as a result of the mature status of 200mm technology and the rate of conversion of alternative package formats to WLCSP. This creates a dilemma for WLP service providers because adding 200mm capacity continues to require a significant amount of capital. Since 200mm volumes will most likely decline within the next 5 years, it is difficult to justify the purchase of capital when the depreciation term is longer than the anticipated life cycle of the product.

A new manufacturing method known as FlexLine has been developed to produce a wafer level package that severs the link between wafer diameter and wafer level packaging methods. The new manufacturing method is wafer size agnostic, so one manufacturing module can produce fan-in, fan-out, and 3D fan-out products regardless of the incoming wafer size. The same bill of materials, manufacturing methods and manufacturing location can produce wafer level packages from any size silicon wafer. Since the manufacturing module is wafer size agnostic, there is no risk of capital for investment in the manufacturing infrastructure. A change in loading between 200mm, 300mm, and 450mm wafers does not adversely affect the utilization of the manufacturing module. This presentation will describe the new manufacturing module approach and the results of process characterization for products produced in the module.

The FlexLine process enables new advanced wafer level packages otherwise unattainable with conventional manufacturing methods. This paper introduces two packages; WLCSP+ and encapsulated WLCSP (eWLCSP) product.

WLCSP+ utilizes the FlexLine process flow with advanced dielectric materials for improved reliability as well as low temperature process. WLCSP+ is capable of 10um via opening size with 10um cured dielectric material thickness on 12" wafers. It can also be thinned down to less than 150um by the backgrind process. The unique process flow, component level and board level reliability test results for this new package will be presented.

eWLCSP has a thin protective coating applied to all exposed silicon surfaces on the die. The applied coating protects the silicon and fragile dielectrics, and prevents handling damage during dicing and assembly operations, effectively providing a durable packaged part in the form factor of a WLCSP. Another unique advantage of eWLCSP is the silicon (Si) die are diced with a mechanical blade before the reconstitution process and actually go through a kind of "burn-in" test after running through the reconstitution, RDL build-up and solder bumping process before final wafer level test.

This paper discusses the key attributes of the new packages as well as the manufacturing process used to create them. Wafer final test, reliability test and qualification results are to be presented and compared to conventional WLCSP products along with analyzing the improvements in package reliability and performance.

Improving the Conventional WLCSP Structure

The wafer level chip scale package (WLCSP) was introduced in the late 1990's as a semiconductor package wherein all manufacturing operations were done in wafer form with dielectrics, thin film metals and solder bumps directly on the surface of the die with no additional packaging [1]. The basic structure of the WLCSP has an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides and back of the die. The WLCSP is the smallest possible package size since the final package is no larger than the required circuit area. The number of WLCSP used in semiconductor packaging has experienced significant growth since its introduction due to the small form factor and high performance requirements of mobile consumer products.

Although WLCSP is now a widely accepted package option, the initial acceptance was limited due to concerns with the Surface Mount Technology (SMT) assembly process and the fragile nature of the exposed silicon inherent in the package design. Assembly skills and methods have improved since the introduction of WLCSP, however, damage to the exposed silicon remains a concern. This is particularly true for advanced node products with fragile dielectric layers. One method commonly used to improve die strength and reduce silicon chipping during assembly is lamination of an epoxy film on the back of the die. By the nature of the backside lamination process, the uncoated sides of the die continue to be exposed after dicing the wafer and the silicon continues to be at risk for chipping, cracking and other handling damage during the assembly process.

A new process has been developed to provide five-sided protection for the exposed silicon in a WLCSP. The ability to apply a protective coating to all the exposed die surfaces in a WLCSP is based on an existing high volume manufacturing flow developed for fan-out products known as embedded Wafer Level Ball Grid Array (eWLB). Unlike conventional WLP, the first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Although this is commonly done for other semiconductor package formats, it has not been practiced for conventional WLCSP. Following singulation, the diced silicon wafers are then reconstituted

into a standardized wafer (or panel) shape for the subsequent process steps as shown in Figure 1.

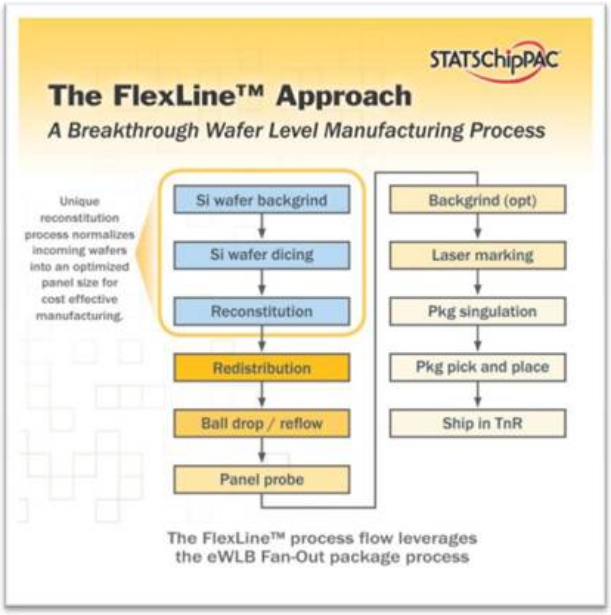


Figure 1. The FlexLine Process Flow

The reconstitution process as shown on the left in Figure 1 includes four main steps.

1) The reconstitution process starts by laminating an adhesive foil onto a carrier.

2) The singulated die are accurately placed face down onto the carrier with a pick and place tool.

3) A compression molding process is used to encapsulate the die with molding compound while the active face of the die is protected.

4) After curing the molding compound, the carrier and foil are removed with a de-bonding process, resulting in a reconstituted wafer where the molding compound surrounds all exposed silicon die surfaces.

The eWLB process is unique in that the reconstituted wafer does not require a carrier during the subsequent wafer level packaging processes. The implementation of this process flow into 300mm diameter reconstituted wafers has been described in detail in previous presentations [2].

FlexLine: Breakthrough Manufacturing Method for Wafer Level Packaging

A new manufacturing method called FlexLine™ has been developed to produce a wafer level package that severs the link between wafer diameter and wafer level packaging methods. The new manufacturing method is wafer size agnostic, so one manufacturing module can produce fan-in (FI), fan-out(FO), and 3D fan-out products regardless of the incoming wafer size. The same bill of materials, manufacturing methods and manufacturing location can produce wafer level packages from any size silicon wafer. Since the manufacturing module is wafer size agnostic, there is no risk of capital for investment in the manufacturing infrastructure. A change in loading between 200mm, 300mm, and 450mm wafers does not adversely affect the utilization of the manufacturing module. The process also enables new advanced wafer level packages otherwise unattainable with conventional manufacturing methods. This presentation will describe the new manufacturing module approach and the results of process characterization for products produced in the module. FlexLine seamlessly processes multiple silicon wafer diameters on the same manufacturing line and produces both fan-out and fan-in devices as illustrated in Figure 2. FlexLine provides the ability to scale a device to larger panel sizes for a compelling cost reduction compared to conventional wafer level packaging methods. FlexLine process has been qualified at advanced silicon nodes down to 22nm, ball pitches down to 0.40mm and body sizes as small as 2.5x2.5mm.

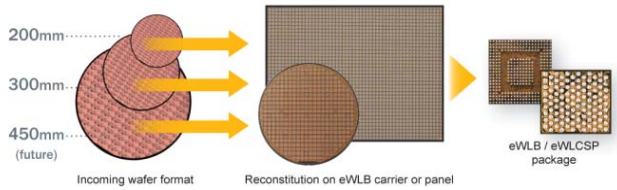


Figure 2: The FlexLine approach can process multiple silicon wafer diameters on the same manufacturing line to produce both fan-in and fan-out packages.

WLCSP+ with Robust Reliability of Advanced Dielectric Materials (ADM)

WLCSP+™ utilizes the FlexLine process flow with advanced dielectric materials for improved reliability as well as low temperature process of ~200°C. So it would be good for temperature-sensitive devices, i.e, SoC with embedded memory. WLCSP+ is capable of flexible design capability so it enables 10um via opening size with 10um cured dielectric material thickness on 12" wafers. It can also be thinned down to less than 150um by the backgrind process. It has same form-factor, fit & function with standard WLCSP but more robust reliability.

Figure 3 is board level reliability of WLCSP+ of 5x4.5mm (0.35mm solder ball pitch, with UBM). It showed over 700 cycles for first failure in TCoB and over 150 drops for its first failure in drop test. There was TCoB performance comparison with standard WLCSP in same body size in Table 1. It has ~20% improvement in TCoB performance of WLCSP+™. It is with enhanced materials properties and more flexible design capability with advanced dielectric materials used in FlexLine. There are several test vehicles which also reported TCoB performance improvement in 15~25% compared to standard WLCSP of 4x4~6x6mm.

(a) (b)

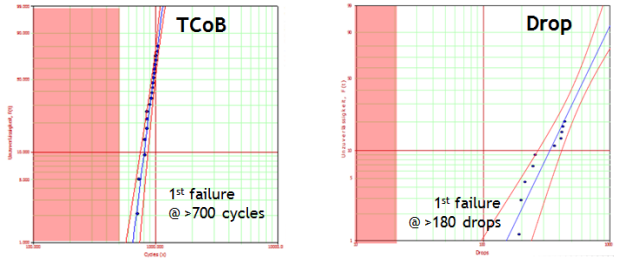


Figure 3. Weilbull plots of board level reliability of WLCSP+ : (a) TCoB and (b) drop test

Table 1. Comparison of TCoB reliability between WLCSP and WLCSP+

	PKG Size	IO	First failure	Characteristic Lifetime
WLCSP	4.8x4.8	144	823	1069
WLCSP+	4.8x4.8	144	1010	1847

Innovative WLCSP with sidewall protection[3]

Using the FlexLine process, a protective coating can be cost effectively applied to the exposed Si surfaces in a WLCSP, thereby addressing the chipping, cracking and other handling damage that can occur during the assembly process. The new WLCSP follows the same process flow as described in Figure 1. Reconstituted wafers are processed with conventional wafer level packaging techniques for the application and patterning of dielectric layers, thin film metals for redistribution and under bump metal and solder bumps. In the final dicing operation a thin layer of molding compound, typically 30um, is left on the side of the die as a protective layer. The back of the die is also protected with molding compound, although with a greater thickness. The result is a new encapsulated WLCSP (eWLCSP™) which has an increased level of durability and reliability over traditional WLCSP designs. The significant benefit of encapsulation is the light and mechanical protection for the bare die. The eWLCSP structure is equivalent to conventional WLCSP with the addition of a thin protective coating on the four sidewalls of the die. A schematic drawing of a typical structure is shown in Figure 4 for greater clarity. Alternatively, the backside molding compound can be removed and the body made thinner with an optional back grind operation without damaging the protective sidewall layer. The remaining sidewall coating will continue to protect the fragile silicon sides of the die during the assembly operation. Figure 5 shows the micrographs of eWLCSP with SEM and optical view.

In FO WLP, the area of the package is increased to allow for placement of redistribution layers (RDL) and solder balls outside of the silicon die area. This allows the die to shrink to a minimum size independent of the required area for an array of solder balls at industry standard BGA ball pitches [4]. It also enables novel multi-die structures, 2.5D structures and 3D structures. In the case of conventional FO WLP die are typically widely spaced to allow for the expanded RDL and bump area and the conventional saw street. In the case of eWLCSP the die are closely spaced, allowing for only the sidewall thickness in addition to a saw street area. The eWLCSP process data presented here was generated with a 300mm round reconstituted panel [5]. The die size was 4.5x4.5mm. The final structure had 2 layers of polymer and 1 layer of plated Cu RDL with the solder ball mounted directly on the RDL without the use of a separate UBM layer.

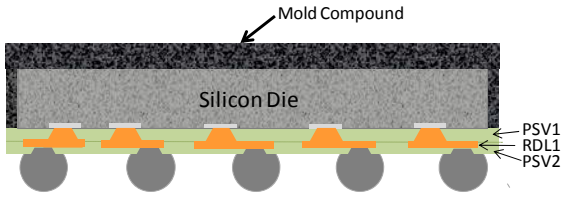
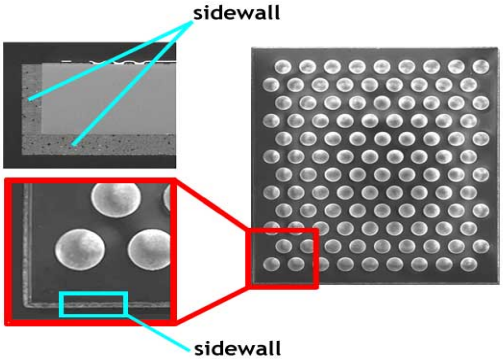


Figure 4. eWLCSP Structure



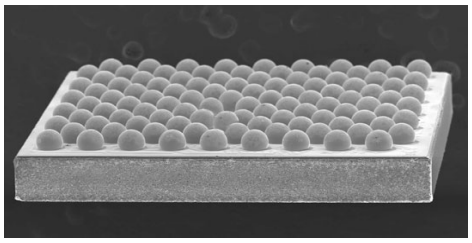


Figure 5. Micrographs of eWLCSP

Structure of the Encapsulated WLCSP (eWLCSP)

Advantages of the Encapsulated WLCSP, eWLCSP [6]

Intuitively, eWLCSP would seem to have a higher cost over conventional WLCSP since there are additional steps required for reconstitution at the start of the FlexLine manufacturing flow. There are two key factors, however, that offset the cost of the additional steps required for the reconstitution to make this a commercially viable process.

(1) Cost-effectiveness

As described above, eWLCSP is fabricated using reconstitution. Good die from the parent wafer are picked and transferred to a (larger) reconstituted carrier. Since the

majority of WLCSP products use 200 mm wafers, reconstitution enables the scaling of the manufacturing process from the 200 mm wafer to the size of the carrier in eWLB technology. This carrier size ranges from 200/300 mm to a larger format like high density (HD) with ~ 20% greater area or Ultra High Density (UHD) with > 300% greater area. The scaling of the manufacturing process with reconstitution far outweighs the cost of reconstitution itself, thereby enabling large net cost reductions. Additionally, the ability to selectively pick good die from the parent wafer presents an additional net cost benefit as most wafers have a less than 100% wafer sort yield. Last but not least, the ability to pool the volume of traditional fan-out eWLB packages seamlessly together with eWLCSP™ packages on the same FlexLine provides important economies of scale. With the three factors stated above, net cost reductions up to 40% over traditional WLCSP front end processing are achievable depending on the original wafer diameter, the carrier format used for reconstitution (300, HD or UHD) and the yield of incoming wafers.

(2) High Quality Solutions

The polymer sidewall structure of eWLCSP all but eliminates mechanical damage such as chipping and cracking that is commonly encountered in traditional WLCSP processing. This serves to eliminate many expensive steps such as back side coating or lamination and complex inspection steps that are currently necessary for standard WLCSP to manage mechanical damage and ensure product quality. More fundamentally, the eWLCSP allows customers to *build in quality by design* vs. using inspection to weed out defects. This has implications for reducing the risk of field failure due to the shipment of marginally defective parts that may escape inspection. As is shown in a later section, the encapsulated eWLCSP structure has also helped to increase the overall die strength by ~ 100% in addition to the mitigation of cracking and chipping defects, making for an overall more robust package.

(3) Investment and Infrastructure – Wafer Agnostic Processing :

In traditional WLCSP processing, the investment and infrastructure for manufacturing are based on the diameter of the incoming wafer. This creates a financial burden to re-tool the manufacturing lines to provide the needed capacity (to meet market demand) as wafer transitions occur (e.g. from 200 mm to 300 mm or from 300 mm to 450 mm in future) while also having to obsolete the existing manufacturing assets. The FlexLine approach for eWLB and eWLCSP effectively decouples the packaging process from the incoming wafer altogether obviating the above-described financial burden resulting from wafer diameter transitions.

(4) Design Friendly – Allows seamless transition from fan-in to fan-out within the same basic package platform:

As noted previously, the standard fan-in WLCSP only works below a certain threshold of I/O density, based on the minimum allowable terminal I/O pitch. - The threshold is ~ 4 I/O /mm2 for a 0.5 mm terminal I/O pitch and ~ 6 I/O /mm2 for 0.4 mm terminal I/O pitch. Small changes in I/O density that commonly occur with changes in Si design, die shrinks resulting from Si node transitions may lead to a given design exceeding the WLCSP threshold, causing the design to "fall off" the WLCSP application space envelope, necessitating a change in packaging POR to traditional substrate- or leadframe-based packages like FBGA, fcBGA, QFN etc. These packages are fundamentally different than WLCSP in terms of footprint, form factor, performance and cost, resulting in a major "reset" in the packaging POR. In contrast, the eWLCSP may be viewed as part of the more universal eWLB platform wherein the aforementioned I/O density transitions can be seamlessly accommodated within the same packaging platform. For designs whose I/O density falls marginally outside the threshold, an additional row of terminal solder balls can be added without fundamentally altering the package structure, form factor or performance.

Reliability of over 6x6mm larger eWLCSP

Robust reliability of 4.5x4.5mm eWLCSP was reported with Component Level Reliability (CLR) and Board Level Reliability (BLR) tests [6].

For reliability tests of larger eWLCSP of over 6x6mm, two test vehicles were prepared, 6x6mm and 8x8mm as shown in Table 2. The eWLCSP process has passed standard reliability tests used in wafer level packaging including CLR and BLR (TCoB and drop test). CLR was completed with the test conditions shown in Table 3.

Table 2. eWLCSP Test Vehicle Details

	eWLCSP size	Mask No.	Solder ball pitch
TV1	6x6mm	3 (without UBM)	0.4mm
TV2	8x8mm	4 (with UBM)	0.35mm

The evaluation results were confirmed by visual inspection and electrical test. No delamination of the protective coating was detected during the CLR evaluation. TCoB was completed and passed 500 cycles with the results shown in Table 4. Result obtained from electrical measurement of daisy chain bump structures demonstrate eWLCSP is comparable to conventional WLCSP product produced with polyimide dielectrics. Drop test was completed and passed the JEDEC requirement of 30 drops with the results shown in Table 4.

4-point bending test was carried out to investigate package level strength. eWLCSP shows over 25% increase die strength compared to WLCSP with sidewall protection. It has significant die strength increase with sidewall protection and optimized backgrinding process.

The Si surface roughness also was measured with AFM (atomic force microscopy). eWLCSP has quite a close Si roughness value to WLCSP. A roughness scan image clearly showed no difference in Si surface roughness between WLCSP and eWLCSP.

The protective sidewall coating is a unique attribute of the eWLCSP package. This protective layer is durable and will prevent silicon chipping on the side of the package and has the ability to protect the silicon during socket insertion for test

[7]. This has been demonstrated through multiple insertion tests on completed products with no observed damage to the protective coating in Table 5.

Table 3. Component Level Reliability Results

Component Level Test	Condition		Status
MSL1	MSL1, 260°C Reflow (3x)	-	Pass
Temperature Cycling (TC) after Precon	-55°C to 125°C	1000 x	Pass
HAST (w/o bias) after Precon	130°C / 85% RH	192 hrs	Pass
High Temperature Storage (HTS)	150°C	1000 hrs	Pass

Table 4. Board Level Reliability Test Results

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103 -40°C to 125°C	Pass
Drop Test	JEDEC JESD22-B111 1500G	Pass

Table 5. Visual Inspection Results after Auto-handler Socket Insertion Test

VM Scan Yield Summary Results	Pre VM Scan	1x Socket Insertion Post VM Scan	2x Socket Insertion Post VM Scan	3x Socket Insertion Post VM Scan
# of Devices Inspected SOU	5000	5000	5000	5000
# of Devices Accepted	5000	5000	5000	5000
VM Yield	100.00%	100.00%	100.00%	100.00%
# of Devices Rejected	0	0	0	0

With these test results along with component and board level reliability results, eWLCSP with additional sidewall protection has demonstrated more robust reliability than standard WLCSP and prevents side chip cracking.

eWLCSP Wafer Level Final Test

An eWLCSP wafer is different from a silicon wafer as the backside of the wafer is mold compound, where it tends to have a much higher warpage level as compared to a similar thickness of a silicon wafer. To enable handling of the eWLCSP wafer using a prober, a few modifications on prober are necessary, these modifications were carried out and successfully demonstrated in a high volume manufacturing environment

Test chuck of the prober was modified for handling of the warped wafers. A progressive and stronger vacuum at the test chuck is necessary to ensure the wafer is properly held flat on the test chunk before testing. The shape of robot handling arms has been modified and the vacuum to these arms were enhanced to ensure proper holding during the transfer of wafer within each module of the prober. One of the key differences between an eWLCSP wafer and silicon wafer is the wafer ID marking on the wafer. For an eWLCSP wafer, the ID marking is on copper surface which makes it look entirely different under the prober's OCR (Optical character recognition) reader. Hence, modification on OCR reader is required to enable reading of wafer ID. Furthermore, in alignment with eWLCSP assembly process, whereas they use modified FOUP (Front Opening Unified Pod) in processing the wafers, the prober software is required to be modified accordingly, so that to accommodate the differences. Figure 6 shows pre-aligner station where the wafer notch is detected and wafer ID is read of eWLCSP carrier.

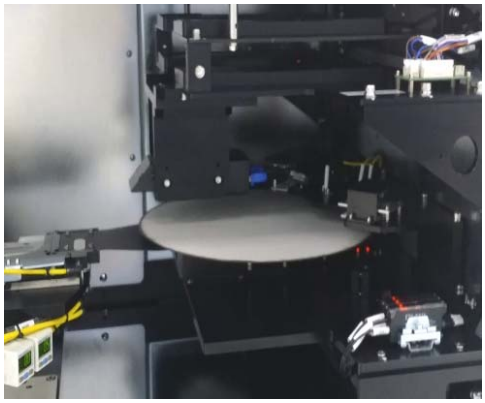


Figure 6. Pre-aligner station where the wafer notch is detected and wafer ID is read of eWLCSP carrier in prober system in FlexLine

Wafer level testing of eWLCSP has been proven with noticeable advantages, such as higher test cell utilization and better first pass yield, which resulted in overall cost reduction of testing these packages. Wafer level testing offers a short index time, especially for high parallel testing. This is mainly due to the indexing from one touchdown to next, where it only involves a small movement within the wafer compared to the pick and place handler which has a high index time. Indeed, this short index time characteristic is most suitable for eWLCSP devices testing, especially for small package sizes, short test times and high parallelism test requirements. Besides achieving higher throughput, wafer level testing improves utilization by lowering manufacturing stoppages, such as jamming associated with the handling of small packages.

Wafer level testing improves the first pass yield by utilizing the visual alignment system, which is standard on a prober. Using camera and vision technology, the socket pins alignment to the package bumps can be highly accurate and repeatable, thus the first pass test yields for wafer level testing are significantly higher. Figure 7 shows indexing process of eWLCSP carrier. Besides providing better and more accurate contacts using vision technology, the prober utilizes its auto socket cleaning feature to improve test yield, whereas this auto cleaning feature is an inline process that minimizes test cell down time and eliminates operator labour needed for manual cleaning. Furthermore, wafer level testing also reduces the tooling and hardware costs. In contrast to pick and place handlers which require a new change kit for every different package size, using a prober to handle wafer level testing eliminates the need to change kits and thus reduces the overall manufacturing cost.

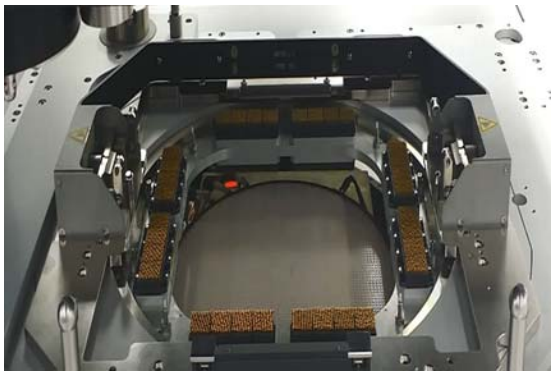


Figure 7. Indexing of eWLCSP™ carrier in wafer test of FlexLine™

Conclusions

Growing demand for WLCSP in a range of advanced mobile products is driving the need to cost effectively reduce risk of cracking, chipping and handling issues before or during the SMT assembly process. This is particularly true for advanced node products where the die is very thin and dielectric layers are extremely fragile. WLCSP+ and a new encapsulated WLCSP (eWLCSP) has been developed and manufactured using a proven manufacturing method known as FlexLine. WLCSP+ is capable of low temperature process and flexible design capability. It also has same form-factor, fit & function with standard WLCSP but more robust board level reliability.

The mechanical sidewall protection that is now possible in eWLCSP devices resolves the problem of silicon damage during the assembly process and provides a path to significant cost savings for customers as the manufacturing panel size is increased. The same manufacturing line can process eWLCSP products regardless of the incoming wafers size and 450mm wafers can easily be accommodated for the encapsulated WLCSP process once the service is required by the customers.

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