# “Development of Exposed Die Large Body to Die Size Ratio Wafer Level Package Technology”

**by**

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**Abstract**

Traditionally fan out wafer level package technology has been associated with lower power, smaller body sizes (typically < 8mmx8mm), small body-to-die size area ratios (<2) and fine pitch BGAs (0.4mm or less). This work extends this technology to larger body sizes up to 13mm x 13mm, higher powers, > 5W, and larger body-to-die size area ratios up to 10.5. It is shown that such packages can be readily manufactured in a 300mm wafer format with yields exceeding 99% and final package warpage < 75um. Further, data is presented showing that 10mm x 10mm packages with a body to die area ratio of 6.25 are compatible with moisture sensitivity level 1, and easily pass 2000 temperature cycle (-55C to 125C air to air) and 288 hr uHAST. That is to say they have reliability that is compatible with that required for all storage and communications applications. Larger package sizes, up to 13mm x 13mm, and body-to-die area ratios, > 10, have also been demonstrated. However, failures in extended temperature cycle were found in these larger packages. All of the failures were due to pre-identified package design flaws that violated well established rules. This indicates if such packages were designed with no rule violations then they would meet the reliability requirements needed for communications and storage applications.

**Introduction**

Although there have been significant challenges for silicon technology to follow Moore's law, leading some to predict its demise, the industry has been able to overcome these challenges and appears ready to continue developing solutions for the challenges at least for the foreseeable future. As such integrated circuits (ICs) continue to move towards finer feature sizes and increased functionality. This drives more die and package I/O with higherpower densities than packages designed andmanufactured in previous generation technology nodes. Further, mobile devices are driving smaller form factor ICs with renewed pressure to reducepackage thickness. The combination of these forces has driven the development of a varietyof chip scale packagesolutionsincluding wafer level packages (WLP), dual row quad flat pack packages (DRQFN), flip chip -chip scale packages (fcCSP), and fan out wafer level packages (FO-WLP).

FO-WLP is an emerging package technology platformthatprovides opportunities for extremely thin, small foot print, high I/O density packages with electrical performance rivaling many of the low-to mid-range fcCSPs and exceeding that for the large majority of lead frame wire bond package technologies [1]. FO-WLP technology has traditionally been associated with lower power, smaller body sizes (typically < 8mmx8mm), small body-to-die size ratios (<2) and fine pitch BGAs (0.4mm or less). However, recent advancements of this technology include demonstrations of side by side multi-chip module (MCM), Package-on-Package (POP), 2.5D, and 3D configurationswhich seem to indicate such limitations may not be fundamental technologybarriers, but rather manufacturing and materials challenges that are waiting to be solved. [2]

To increase the breadth and type of markets that this technology can be applied to, improvements in thermal performance and larger body-to-die area ratios are required. These market segments impose requirements such as: BGA pitchesas large as 0.65mm and in some cases 0.8mm; > 5watts power dissipation; body sizes of 15mm or larger; and body-to-die size ratios of >10. Furthermore, some of these markets segments also require a minimum lifetime of 10 years. In this paper, our results on the development and qualification of an exposed die fan-out wafer level package technology with body-to-die aspect ratios of >10 and body sizes up to 13mm x 13mm are presented.

**Process Development and Control**

A schematic of the package technology developed in this work is shown in Figure 1. The package contains a 250um thick, 16mm$^2$ die embedded in a mold compound with 2 layers of package routing connected to 0.25mm diameter, 305SAC BGA solder balls. The die are designed into a 40nm silicon node technology. The maximum package height is 0.68mm and the number of I/O was > 200. Two sizes of packages were used for the work, i) 10mm x10mm with a BGA pitch of 0.5mm ; and ii) 13mm x 13mm with a BGA pitch of 0.65mm. Thus, the body-to-die area ratios were 6.25 and 10.5 respectively. The same die was used for both packages; however, the package routing was different. The large body-to-die ratio tends to drive to higher package warpage making it difficult to meet JEDEC and IPC requirements. [3]

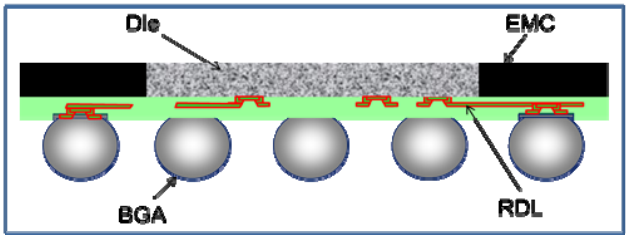


Figure 1: Schematic of an exposed die FO-WLP

Although back side mold compound on the die helps to mitigate the difficulty in meeting the warpage specifications, the 5W power dissipation requirement for these market

applications prevents, as discussed next, the use of this warpage mitigation approach from being implemented. The thermal simulation done for both package sizes using the design constraints and thermal boundary conditions of the market segment this device is targeted for indicate a mold compound thickness greater than 35um will prevent the package from meeting the 5W requirements, Figure 2. In this simulation, the system configuration and restriction on air flow were modeled with 3-D finite element model, 3w/mK TIM material, a die size 4mm x 4mm in a 10mm x 10mm package.After assessment of variation in die performance at all silicon and FO-WLP process corners, as well as the system corners, it was concluded that an exposed die format was needed to meet the thermal requirements.

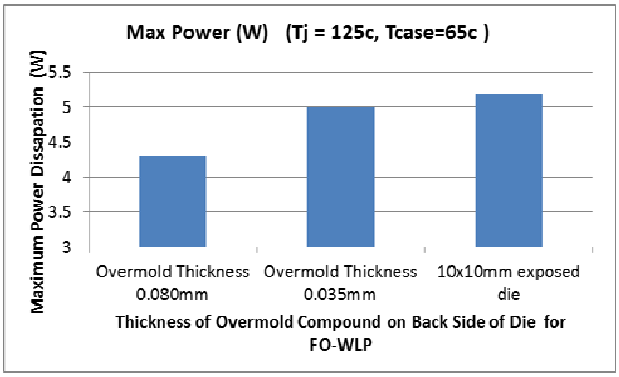


Figure 2: Dependence of max power dissipation on mold thickness on back side of die in a 10mm x 10mm FO-WLP

In this work the FO-WLP were made in 12" diameter format. An overview of the process flow is given in Figure 3. Known good die are picked from the diced wafer and placed active side face down onto a carrier array at predefined x, y positions. The gap between each die is used to create the FO-WLP routing and BGA connections. There were approximately 40% fewer die and thus packages for the 13mm x 13mm package than for the 10mm x 10mm package, driven completely by area considerations. The carrier wafer has a commercially available adhesive film on it which is used to hold the die in place at pick and place as well as during the molding process. After the carrier wafer is fully populated with die, the entire carrier wafer is overmolded with a commercially available mold compound. Following mold compound cure, the carrier is removed from the composite wafer, die plus mold compound, exposing the active side and bond pads for further processing. The package routing is then completedusing standard spin deposition of interlevel dielectrics, lithography, and Cu plating technology. First, dielectric layer 1 is spun on the composite wafer and patterned, opening up the bond pad regions of the die. Cu is deposited and patterned, followed by a second layer of dielectric and metal. The final passivation layer is then deposited and patterned. Note the final passivation layer in the FO-WLP is equivalent to a solder mask in a standard substrate based technology. The wafer is then fluxed after which BGA balls are placed on each pad and reflowed. Because the product thermal requirement can only be met with an exposed die back side configuration, the back side mold compound is then removed.The fully processed carrier wafer, which is now a wafer array of packages, is then diced creating individual packages. The packages are then tested and packed into dry bags ready for shipment.

Figure 4 shows a cross section of a 13x13mm FO-WLP test vehicle. The die, mold compound (EMC), BGA, Cu RDL layers and dielectric RDL layers are identified in this figure. As shown all interfaces are intact with no signs of delamination, separation or cracking of the different materials or interfaces. Figure 5 is a micrograph of the BGA side of both the 10mm x 10mm and 13mm x 13mm packages. Also show is the approximate position and size of the die.

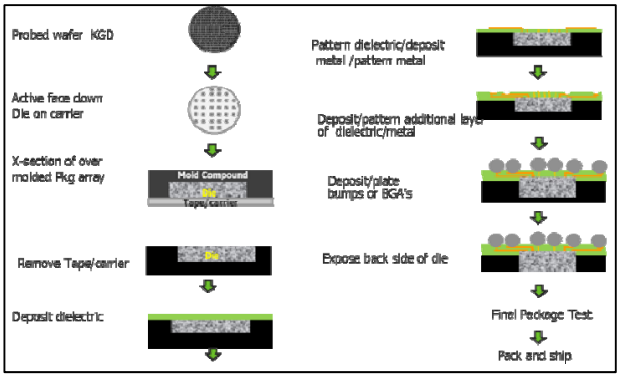


Figure 3: Overview of process flow for the devices used in this work

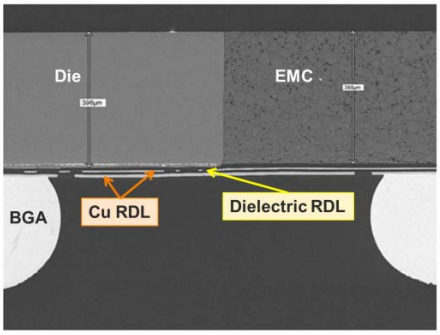


Figure 4: Cross section of a 13x13mm FO-WLP test vehicle

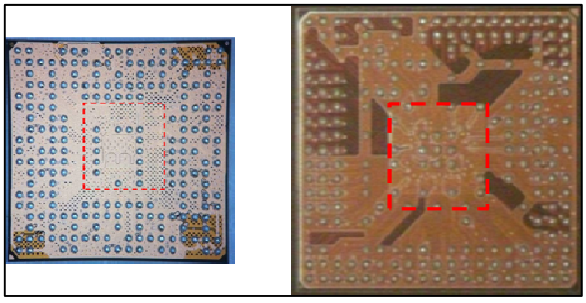

Figure 5: Micrograph of 10mm x10mm and 13mm x 13mm packages; outline of approximate position of the die are shown as the red dotted box.

The body-to-die area ratios, 6.25-10.5, used in this development along with the exposed back side construction and 2 layers of routing were substantially outside of the established design and process window for FO-WLP. As such significant development was needed to establish a process witha well-controlled-,reproducible-, and predictable-die shift and composite wafer warpage, as these two physical attributes largely influence interconnect patterning and wafer handling both of which ultimately control the overall package yield. Initial builds made with the previously "established" processes and materials led to package yields that were less than 90%, clearly not an acceptable yield for low cost, high volume manufacturing. Subsequent process and materials development and optimization led to yields approaching or exceeding 99%. It was thus concluded that this type of package technology is capable of competing on a yield basis with well-established traditional wire bond and flip chip package technology even for the packages developed in this work which have somewhat extreme body-to-die ratios in an exposed die configuration.

In addition, the yield as measured by electrical testing, control of the final package dimensions (X, Y and Z) and warpage is critical. Figure 6is a plot of the dimensions (X, Y and Z) and warpage of the 10mm x 10mm packages.Similar behavior was observed for the 13mm x 13mm packages, however, the number of 13mm x 13mm FO-wafers and packages made was significantly smaller than made the number of 10mm x 10mm FO-wafer and packages. Thus, conclusions about dimensional (X, Y and Z) and warpage control are somewhat less well-founded in data for the 13mm x 13mm package than for the 10mm x 10mm package. As a result we restricted this discussion to the 10mm x10mm package. As shown, for the 10mm x 10mm packages, the package dimensions and wapageare well controlled with warpage being < 50um on average with a three sigma maximum of ~75um which is well below the JEDEC and IPC requirements for this package and BGA size.

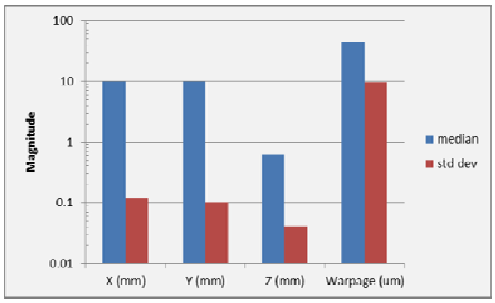


Figure 6: Median and standard deviation of X, Y, and Z dimensional control and of final package warpage at room temperature for the 10mm x 10mm package

**Reliability**

The reliability work is summarized in Table 1. All devices were tested then subjected to Moisture Sensitivity Level (MSL)exposure followed by 3x-260C reflow and re-tested. The 10mm x 10mm packages were subjected to MSL1 and the 13mm x 13mm to MSL3. The 10mm x 10mm packages used in cell 1 were taken from twodifferent FO-wafer builds whereas those in cell 2 were taken from 4 wafer buildsmade some 3-4 months after those in cell 1. All 13mm x 13mm devices were taken from one wafer build.Following MSL/reflow exposure, devices from each package type were then subjected to either temperature cycle JEDEC condition B (-55C to + 125C air to air) up to 2000 cycles or to unbiased Hast (uHAST- 130C/85%RH) up to 288hrs [4]. Periodically the packages were removed from the stress tests and electrically characterized. All electrically good devices were then placed back into the stress test chamber for additional aging. The temperature cycling and uHAST testing duration wasextended with the intent of insuring the packages were not close to end of life after exposure to the more conventional JEDEC tests. The thesis being, exposure to extended temperature cycles and/or time in uHAST conditionswould either show where the ultimate failure lifetime would be or if no failures were foundindicate the packages are significantly more robust than required for use in high reliability environments with no failures .

| Cell | Package Type | MSL | TCB (Cycles-#fail/#tested) | | | | uHAST (hr-#fail/#tested) | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | 500 | 1000 | 1500 | 2000 | 96 | 192 | 288 |
| 1 | 10mm x 10mm | 0/320 | 0/160 | 0/160 | ------- | ------- | 0/160 | 0/160 | ------- |
| 2 | 10mm x 10mm | 0/660 | 0/330 | 0/330 | 0/330 | 0/330 | 0/330 | 0/330 | 0/330 |
| 3 | 13mm x 13mm | 0/94 | 0/47 | 1/47 | ------- | 32/47 | 0/47 | 0/47 | ------- |

Table 1: Summary of qualification testing done for 10mm x 10mm and 13mm x 13mm packages(10x10mm device has 0.5mm BGA pitch, 13x13mm device has 0.65mm BGA pitch)

As shown, failures were not observed in either cell in any of the stress tests independent of duration for the10mm x 10mm packages. Given that the devices used for this test were taken from a total of 6 wafer builds over a multiple month time period, the sample sizes used in each test and the fact that TCB and uHAST stress tests were extended 2x and 3x respectively beyond standard JEDEC recomendations, it is conclude that such packages are very reliable and thus compatible with all storage and communications applications.

Although the 13mm x 13mm package easily passed MSL3 and extended uHAST, ~2% (1/47) of the devices failed after exposure to 1000 temperature cycles, and ~ 70% (32/47) of the devices failed after 2000 temperature cycles. The failure site and mechanism was similar for all 32 failures. Figure 7shows two micrographs of the failure site. The failure is a result of metal fatigue of a metal 1 trace near the die edge at the die to mold compound interface. This particular trace is also under the BGA and BGA pad in metal 2. Placement of the BGA in this location is and was a design rule violation which was identified in the design stage. It was flagged as a potential weakness in the design that could be susceptible to temperature cycling induced failure. In additionthe RDL stack used in this work was designed for solder balls compatible with BGA pitch $\leq$ 0.5mm, note for 0.65mm pitch as was used for the 13mm x 13mm package used here. Given larger diameter BGA solder ballsdrive higher localized stresses in lower level structures, this was also flagged as a potential reliability issues in the design stage.However, because there was a need to make the 13mm x 13mm FO-WLP pin to pin compatible with a 2 layer flip chip version of the same device, the design rule

violationsand potential reliability risks/failure modes were noted, but the design proceeded with no changes to accommodate the rule violations. Thus it was understood at the outset of the program that the 13mm x 13mm package could be susceptible to failure in temperature cycling and/or other qualification stress test. Given all temperature failures were related to the design violations, it is concluded that FO-WLP designs with body-to die ratios≤10.5, that follow the existing design rules, have a high probability of meeting and, in fact, exceeding the JEDEC temperature cycling requirements.

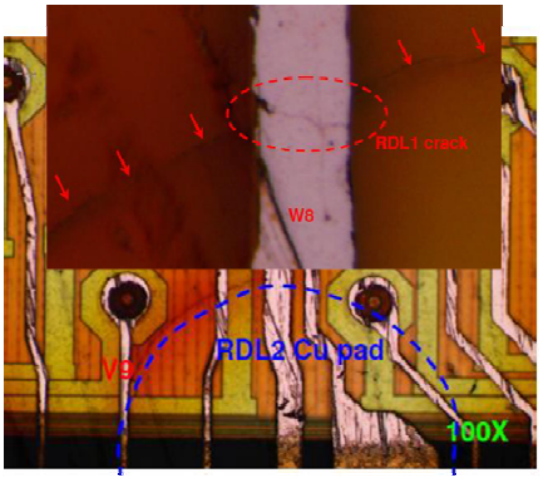


Figure 7: Micrographs representative of all 13mm x 13mm TCB induced failures.

**Conclusions:**

Traditional fan out wafer level package technology has been associated with lower power, smaller body sizes (typically < 8mmx8mm), small body-to-die size area ratios (<2) and fine pitch BGAs (0.4mm or less) package designs. The work presented here extends this technology to larger body sizes, up to 13mm x 13mm, higher powers, > 5W, and larger body-to-die size area ratios,up to 10.5. It is shown that such packages can be readily manufactured in a 300mm wafer format with yields exceeding 99% and final package warpage < 75um. Further, data is presented showing that 10mm x 10mm packages with a body to die area ratio of 6.25 are compatible with moisture sensitivity level 1, easily pass 2000 temperature cycle (-55C to 125C air to air) and 288 hr uHAST. That is to say they have reliability that is compatible with or exceeds that required for all storage and communications applications. Larger package sizes, up to 13mm x 13mm, with body-to-die area ratios in excess of 10, have also been demonstrated, however, failures in extended temperature cycle were found. All of the failures were due to pre-identified package design flaws that violated well established rules. This indicates if such packages were designed with no rule violations then they would meet the reliability requirements needed for communications and storage applications

**Acknowledgments**

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