Ultra Thin Substrate Assembly Challenges for Advanced Flip Chip Package

by

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Abstract
Advanced semiconductor packaging requirements for higher and faster performance in a thinner and smaller form factor continues to grow for mobile, network and consumer devices. While the increase in device input/output (I/O) count is driven by the famous "Moore's Law", the packaging industry is experiencing opposing trends for more complex packaging solutions while the expected cost targets are in a downward direction.
Demand for high speed flip chip packages create an opportunity for highly integrated, multi-chip modules (MCM's) and 2.5D/3D silicon (Si) interposer packages which are emerging very slowly now due to the higher costs often associated with infrastructure and supply chain challenges before a technology is mature. Achieving both increased margins in the power delivery and increased functionality in next generation high speed applications requires extremely efficient, low loss package designs with an ultra thin core or coreless substrate with fine line and space. As the substrate gets thinner, it becomes very flexible and one of the biggest assembly challenges for ultra thin coreless substrates is to keep the substrate flat during the assembly process and maintain yield targets. Other issues with thin substrates are more or less related to post assembly such as handling, long term package reliability and functionality in the application field. The work presented in this paper describes key factors for mitigating several assembly related issues in the manufacturing line, including package warpage/coplanarity, and selecting the optimum processes and materials for such ultra thin coreless substrate flip chip packages with high assembly yields.

A very comprehensive design of experiment (DOE) is being carried out to achieve the objective of the work. A test vehicle has been designed using a flip chip package with ultra thin coreless buildup substrate utilizing various assembly materials and processes. More work will be carried out to expand the scope of the technology for multi chip module (MCM) die and 2.5D integration.

Keywords: flip chip, ultra thin substrate, recon, assembly, warpage.

Introduction
As chip technology gets more and more advanced along with the aim toward product miniaturization, the need to reduce the chip package form factor while increasing chip performance has become critical to enabling more advanced chip technology and product miniaturization. Traditional flip chip packages are made with multi-layer build up substrates. However, conventional cored substrates have lots of through holes in the core, creating obstacles to high speed and high frequency applications. The curvature and unevenness of the core laminate have become the limiting factor in achieving the fabrication of high density substrates. Moreover, some applications require very thin substrates with robust routing density. Cost is the other parameter which cannot be neglected at the end of the day. Considering all the challenges, a new enabling technology is needed to address the issues. The ultra thin substrate is one such enabler for more advanced chip technology and product miniaturization which potentially can be used for thin packages with homogeneous as well as heterogonous integration (system-in-package or SiP). According to some literature [1-3], the high density thin film substrate can extend SiP technology to a new version of a thinner and higher performance package. The challenges facing the ultra thin substrate along with suggestions for overcoming these challenges will be presented.

Ultra Thin Substrate Design
The salient feature of an ultra thin substrate is its thickness which can be an order of magnitude thinner than normal flip chip laminate or build up substrates. Figure 1 shows a typical ultra thin substrate in the market. With such a thin film based substrate, the chip package height can be reduced significantly which enables the adoption of high speed flip chip for thin application areas. However, there is one major drawback from having such a thin substrate and that is excessive warpage of the bare substrate. Figure 2 shows a 17X17 mm body size bare ultra thin substrate moiré warpage 3D plots at room temperature. The plots show that the bare ultra thin substrate warpage is much higher than conventional flip chip substrates. Figure 3 shows examples of the bare ultra thin substrate warpage. Due to the bare ultra thin substrate's excessive warpage, the use of the ultra thin substrate presents significant assembly challenges that must be overcome before this substrate can be adopted for mainstream package applications.

Figure 1: Typical ultra thin substrate (IMEC; courtesy: www.sciencedaily.com)

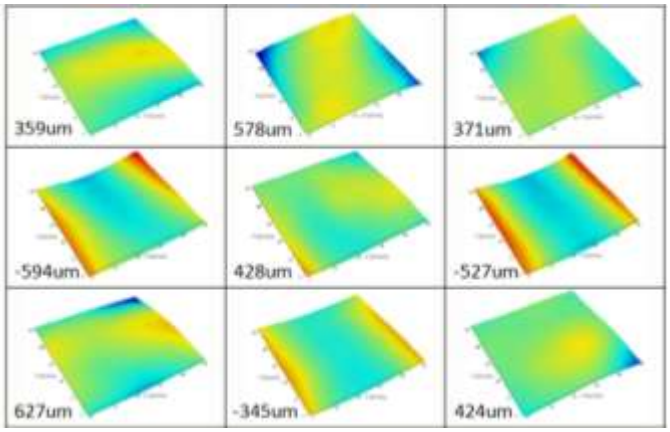


Figure 2: 17X17mm body size ultra thin bare substrate warpage data at 25^0C

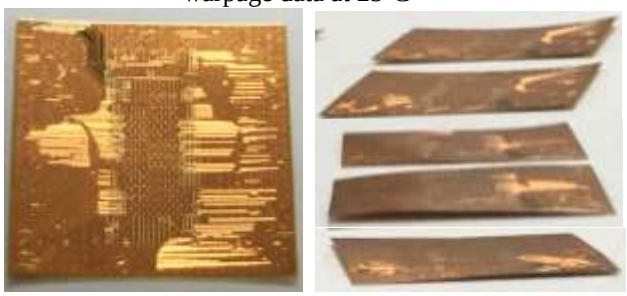


Figure 3: Optical pictures of ultra thin bare substrate

Test Vehicle (TV)

In this device design, a 17X17mm molded package with 7.25X5.0 mm die size with 40nm silicon was used with full array bumps at 150um pitch. The design has 0.65 mm BGA pitch with over 475 solder balls in a 6 layer, very thin build up film type substrate. Total substrate stack up thickness was about 65um. In order to protect the ELK layer of the die, and minimize the package warpage, a low coefficient of thermal expansion (CTE) build up material was used in the design. Figure 4 shows the cross sectional view of a typical fcFBGA package.

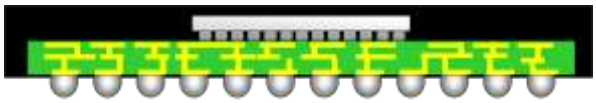


Figure 4: Cross sectional view of ultra-thin fcFBGA TV

Assembly Process

Packages were manufactured at several development phases described below.

Feasibility build: One of the critical phases in manufacturing was the feasibility building with the down selected mold compound materials. Several key assembly process parameters were reviewed. A comprehensive DOE with assembly process parameters was conducted.

A new assembly process named Recon® which is Broadcom Limited's proprietary technology that is available for licensing. The Recon technology involves the reconstitution of singular substrates placed on a polyimide tape fixed to a window carrier which is then laminated, over-molded and sawn to produce individual chip packages. Figure 5 shows the Recon technology process flow and Figure 6 shows the singular ultra thin substrates placed on the polyimide tape fixed to a window carrier prior to the reconstitution process. With the Recon technology, minimizing the substrate backside surface flatness helps to prevent mold bleeds onto the substrate backside. Figure 7 shows the TV 1 ultra thin substrate backside surface flatness measurements. Although all flatness measurements are less than the 5 um specification limit, it will be shown later that the excessively high bare ultra thin substrate warpage becomes the dominating factor for mold bleeds to the point of negating the effect from the substrate backside surface flatness.

Figure 5: Recon® technology process flow

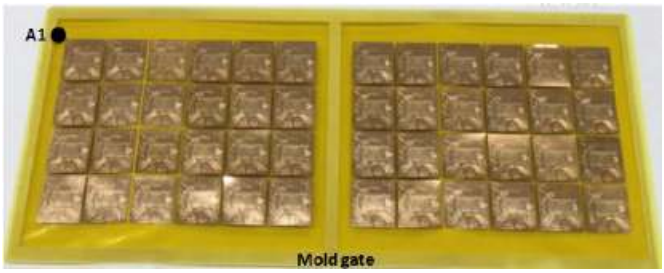


Figure 6: Singulated ultra thin substrates placed on the polyimide tape fixed to a window carrier prior to the reconstitution process.

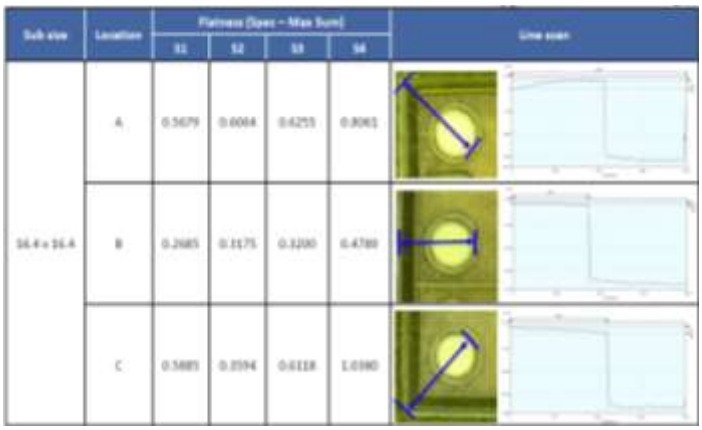


Figure 7: TV 1 ultra thin substrate backside surface flatness data

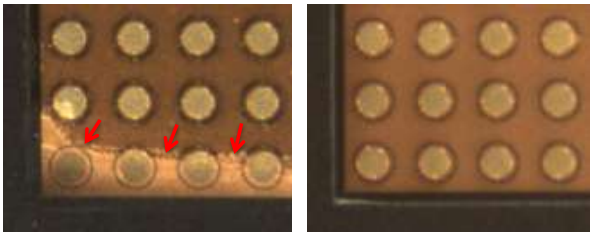
Test Vehicle 1 (TV 1) Evaluation and Results

Three evaluations were conducted with the TV 1. All three evaluations initially experienced some level of mold bleed issues, but the occurrence decreased with subsequent evaluations as shown in Table 1. The decrease in the mold bleed occurrence with subsequent evaluations is due to the tooling and process improvements made as indicated in the 'Feature' column of Table 1. The mold bleed is caused by the excessive substrate warpage which tends to create gaps between the polyimide tape and the substrate bottom side at or near the substrate corners. Examples of these gaps observed after the Recon technology's lamination process from the TV 1-1 evaluation are shown in Figure 8 while Figure 9 shows the TV 1-1 evaluation mold bleed examples. Even if no gaps had been observed prior to the mold process, the large bare ultra thin substrate warpage changes going from room temperature to the mold pre-heat temperature and back to room temperature weakens the polyimide tape-to-substrate adhesion leading to gaps at or near the substrate corners. Bare incoming substrates were thoroughly investigated and bare substrate warpage at mold temperature conditions were measured to understand the root cause for mold bleeding. Figure 10 shows the bare substrate and post lamination process with thermal moiré warpage data. Very high warpage observed from high temperature (175^0C) to room temperature.

Eval	Feature	*Mold bleed on pad*
TV 1-1	Applied new pick & place nozzle.	*30/96 or 31.2%*
TV 1-2	Applied a larger lamination size tool.	*6/48 or 12.5%*
TV 1-3	Applied improved transfer pressure and pre-heat time.	*5/44 or 11.3%*

Table 1: Mold bleeds evaluation results

Figure 8: Gap between substrate and tape observed after the lamination process from the TV1-1 evaluation



Mold bleed on pad No mold bleed on pad

Figure 9: Examples of mold bleed in the substrate pad

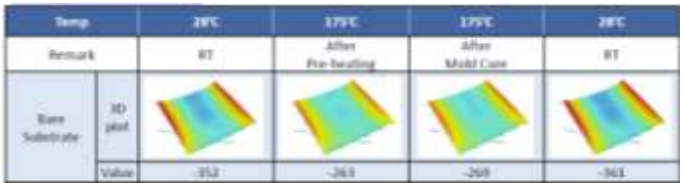
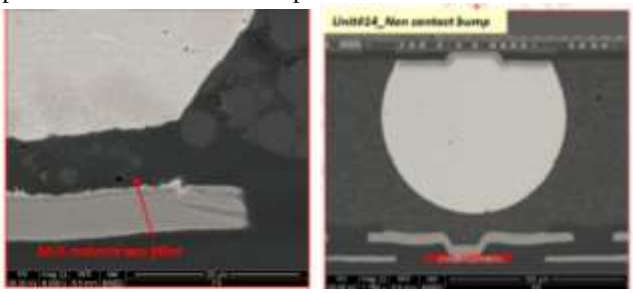


Figure 10: Ultra thin substrate thermal moiré warpage plots for room-pre-heat-room temperature transitions

Several other issues were encountered in the development processes. One issue is the brittle separations at the bump-to-bump pad interface after solder joint formation resulting in the MUF material filling in the separation area. Another issue is the non-wets likely due to the high substrate warpage during the chip attach reflow process. Figure 11 shows brittle separation and non-wet examples.



(a) (b)

Figure 11: (a) A brittle separation at the bump-to-bump pad interface with the MUF material filled in and (b) a non-wet

Test Vehicle 2 (TV 2) Evaluation and Results

TV 2 uses the same 17 x 17 mm fcFBGA package as TV 1 except the maximum package and substrate thickness for TV 2 are respectively 1.1 and 0.052 mm compared to 1.5 and 0.065 mm for TV 1. Like TV 1, TV 2 also used the MUF and Recon® process. Much thinner die (150um thick Si) was used in TV 2 whereas TV 1 die thickness was 330um. Various EMC and PI types were used in the evaluation DOE. TV 2 with the evaluation matrix is shown in Table 2. All legs in the evaluation have mold bleeding on pad and all legs, except legs 4 and 6, have mold bleeding into ball pad area. Based on the results, the mold compound does not appear to be a significant factor to the mold bleed. However, the legs with the PI-B polyimide tape appear to have little or no mold bleeding into ball pad area. Further evaluations are required to verify the effect of the PI-B polyimide tape on the mold bleed.

Leg	PI tape	EMC	Sample size	Mold bleeding into ball pad area
1(con)	PI-D	EMC-U	48	23 / 48 (47.9%)
2	PI-B	EMC-U	48	6 / 48 (12.5%)
3	PI-D	EMC-C	48	16 / 48 (33.3%)
4	PI-B	EMC-C	48	0 / 48 (0%)
5	PI-D	EMC-Q	48	12 / 48 (25.0%)
6	PI-B	EMC-Q	48	0 / 48 (0%)

Table 2: TV 2 evaluation matrix

Mold bleed on pad unit mapping in Figure appears to show the mold bleed on pad units from the TV 2 evaluation matrix are randomly distributed on the strip with the mold air vent at

the top of the strip and the mold gate at the bottom of the strip.

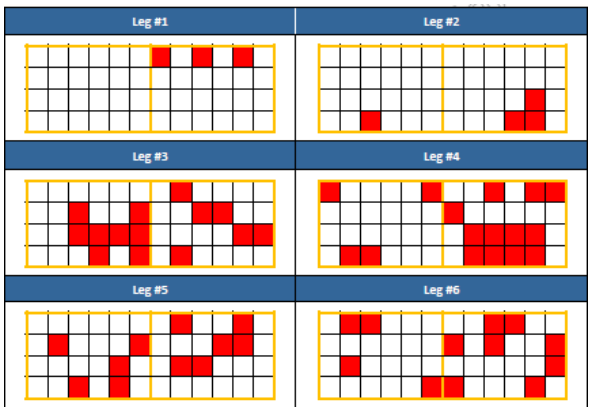


Figure 12: Mold bleed on pad unit mapping of the mold bleed units from the TV 2 evaluation matrix

Strip warpage measurements of the legs from the TV 2 evaluation matrix are within the 7 mm specification as shown in Table 3 and Table 3: TV 2 DOE strip warpage data

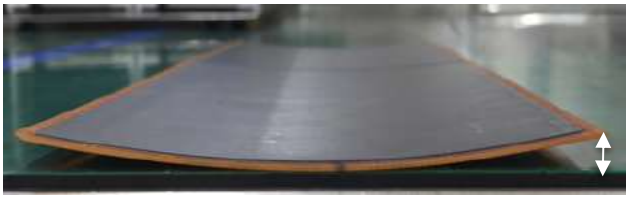


Figure **12** respectively. Strip warpage varies significantly depending on the mold compound or EMC type. Much lower strip warpage with low shrinkage and low CTE mold compound (EMC-C) type. However, the maximum package warpage data at room and high temperatures are shown in Table 13 are much higher than standard spec (100um at any given temperatures). Process control (Cpk) values are not good because the average coplanarity values exceed the 100 um limit. The high coplanarity readings are due to the excessive thin substrate warpage. TV 2 package level coplanarity data are shown in Figure 14.

Leg	PI tape	EMC	Sample size	Strip warpage
1(con)	PI-D	EMC-U	1 strip	6 mm
2	PI-B	EMC-U	1 strip	6 mm
3	PI-D	EMC-C	1 strip	3.5 mm
4	PI-B	EMC-C	1 strip	3.5 mm
5	PI-D	EMC-Q	1 strip	5 mm
6	PI-B	EMC-Q	1 strip	5 mm

Table 3: TV 2 DOE strip warpage data

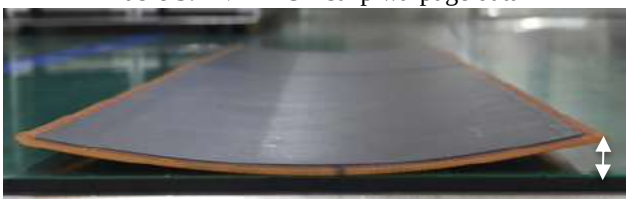


Figure 12: Typical strip warpage shape from TV 2 DOE

Leg	PI tape	EMC	Sample size	Warpage (um)			
				25^{0}C		260^{0}C	
				Max	Avg.	Max	Avg.
1(con)	PI-D	EMC-U	8units	-187	-167	176	154
2	PI-B						
3	PI-D	EMC-C	8units	-144	-117	183	160
4	PI-B						
5	PI-D	EMC-Q	8units	-161	-124	244	226
6	PI-B						

Table 13: Package warpage data at room and high temperatures from the TV 2 evaluation matrix

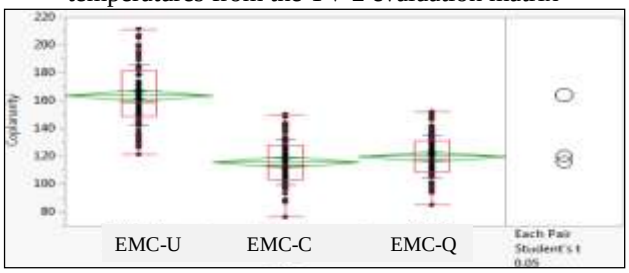


Figure 14: Coplanarity data by EMC type

Besides the mold bleed issue, another major issue found with the TV 2 evaluation is the bump non-wet. Prior to checking for non-wets, SCK performed open-short tests on the TV 2 evaluation units with the results shown in Table 5 and Figure 15 shows the failure mapping. All legs have at least 1 open failure with the open failures randomly distributed on the strip. SCK then performed extensive cross sections at the failed open pins from a few open failed units and found non-wets due to excessive warpage like those shown in Figure 16.

Leg	PI tape	EMC	Sample size	O/S Test		
				Open	Short	Yield
1(con)	PI-D	EMC-U	47	1/47	0/47	97.87%
2	PI-B		46	7/46	0/46	84.78%
3	PI-D	EMC-C	45	6/45	0/45	86.67%
4	PI-B		38	7/38	0/38	81.58%
5	PI-D	EMC-Q	46	10/46	0/46	78.26%
6	PI-B		44	8/44	0/44	81.82%

Table 5: TV 2 O/S results

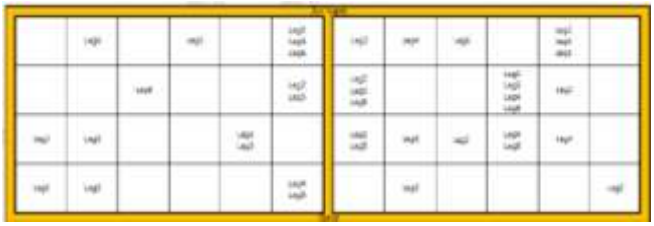


Figure 15: TV 2 O/S failure mapping in the strip

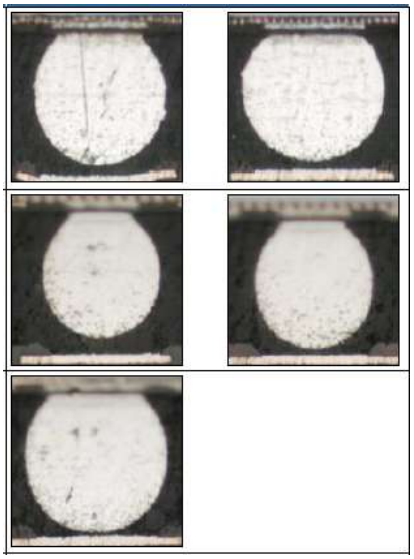


Figure 16: TV 2 non-wets due to excessive substrate warpage

Some of the functionally good parts were also cross-sectioned and check the bump integrity and other anomalies in the package. No bump crack or tearing and EMC crack or separation observed in the picture shown in Figure 17.

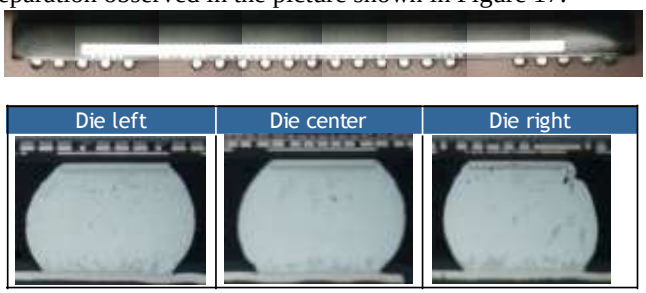


Figure 17: No bump crack or non-wet observed with good units from TV2 DOE

Suggestions for Overcoming Challenges

For the ultra thin substrate to be adopted for mainstream use in flip chip packages, more evaluations are required to overcome two major challenges resulting from the use of this substrate. These two major challenges are mold bleeds and non-wets. Both of these issues are due to the excessive substrate warpage from ultra thin substrate as mentioned several times in the paper. Material and process evaluations need to be carried out to counter the excessive ultra thin substrate warpage. For example, a lamination film material evaluation could be conducted to determine the film material with the optimal substrate-to-tape adhesion to help prevent the mold bleed issue. A chip attach reflow profile evaluation could be conducted to help prevent non-wets. Design modifications to the chip attach jig and window carriers could also be investigated to help counter the excessive ultra thin substrate warpage. Comprehensive assembly process data and reliability data along with optimum bill of materials (BOM) needs to be evaluated prior to technology qualification.

Conclusions

The ultra thin substrate is a promising technology enabler for more advance chip technology and product miniaturization with very fine line/space which potentially can be used for multi die high I/O Si integration such as MCM, 2.5D/3D applications. However, challenges such substrate flatness which results in mold bleeding, non-wets must be resolved before the ultra thin substrate technology can be adopted for mainstream use. The suggested evaluations presented here could help to overcome these challenges in our future work.

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