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## ABSTRACT

As the demands of higher performance, higher bandwidth, and lower power consumption as well as multiple functions increases, the industry is driving advance technology developments in emerging markets, especially in portable and mobile devices to meet these requirements. The utilization of emerging technologies is pushing smaller form factor package designs with finer line width and spacing as well as improved electric and thermal performance and passive embedded technology capabilities. Due to the fast growth in emerging markets for mobile applications, a numbers of wireless devices have jumped to 4G Long Term Evolution (LTE) communication platform and may ramp to 5G generation technology in the next two to three years. In addition, advanced silicon (Si) node (20/16/14nm and below) technology development in mobile applications can pursue the die size reduction, efficiency enhancement and lower power consumption. Based on these demands and evolution of the mobile communication platform, package types become more complicated and have migrated from wirebond packaging to flip chip chip scale package (fcCSP) when higher input/output (I/O) counts are needed. For the purpose of having the shortest interconnection between logic devices and mobile low power double data rate (LPDDR) memory, three-dimensional (3D) package-on-package solutions with flip chip interconnect (fcPoP) has been widely utilized. With the ability to stack a logic processor and memory device in a single package, the utilization of fcPoP is becoming a preferred solution for achieving the best performance and efficiency as well as smaller form factor in the mobile market segment.

Since the industry adopted fcPoP as a dominant package approach to address the mid to high-end mobile market, various fcPoP developments have been widely discussed. Among these fcPoP structures, bare die package-on-package (BD-PoP) and molded laser package-on-package (MLP-PoP) are the most common fcPoP types being utilized in mobile applications today. Challenges in finer pitch memory devices, thinner package profiles, stringent package warpage/coplanarity requirements as well as Surface Mount Technology (SMT) processes are being addressed. This paper reports the BD-PoP and MLP-PoP developments with a 15x15mm package size that achieve the thin profile and warpage/coplanarity targets. Through the result, low profile (total package height less than 1.2mm) solutions for both BD-PoP and MLP-PoP in mobile applications have been fabricated and demonstrated. The warpage/coplanarity control as well as reliability characterization will also illustrated, which shows these architectures are cost-effective 3D packaging solutions for highly integrated, miniaturized and low profile enabling technology.

## INTRODUCTION

With the rapid technology developments in the semiconductor industry, the mobile phone has evolved from a simple communication device to a complicated and highly integrated system with multiple functions and heterogeneous devices. Based on the fast growth in emerging markets for mobile applications, packaging semiconductor devices are becoming more challenging than ever before. Based on these demands and evolution of the mobile communication platform, package types become more complicated and have migrated from wirebond packaging to flip chip interconnect when higher input/output (I/O) counts are needed [1, 2]. To meet the requirement of higher I/O counts, the flip chip chip scale package (fcCSP) has become the mainstream package type for mobile application processors (AP) as well as baseband processors (BB) [3]. However, as the demand of higher performance, higher bandwidth, lower power consumption and smaller form factor are increasingly required in portable mobile devices, standard flip chip packages such as fcCSP are not able to meet these requirements. Hence, 3D package-on-package solution with flip chip interconnect (fcPoP) has been widely utilized to successfully achieve these goals. With the ability to stack a logic processor and memory device in a single package, the utilization of fcPoP is becoming a preferred solution in the mobile market segment. It is well known that fcPoP technology developments are related to the evolution of mobile low power double data rate (LPDDR) memory, requiring lower voltage, lower power consumption and higher transition rates, a significant number of 4G LTE mobile devices are adopting fcPoP with LPDDR3 and are now migrating to LPDDR4 as well as finer silicon nodes (below 20nm). Challenges in finer pitch memory devices, thinner package profiles, stringent package warpage/coplanarity requirements and Surface Mount Technology (SMT) processes are successfully met with fcPoP technology. This paper reports the 3D package developments with flip chip technology, including bare die package-on-package (BD-PoP) and molded laser package-on-package (MLP-PoP) to meet low package profile demands (total maximum package height less than 1.2mm). The adoption of copper (Cu) pillar and the associated Bond-on-Lead (BoL) technology was adopted to provide substrate cost reduction through design rule relaxation as well as bump pitch reduction and performance improvement. Evaluations of different underfill, substrate core materials, die thickness as well as epoxy molding compound (EMC) materials selection were studied not only to meet warpage and coplanarity target but also pass the long term package reliability conditions. The pre-stack technology in MLP-PoP is also illustrated to have better warpage and coplanarity control in the whole package. These results show fcPoP architecture is an enabling technology for highly integrated, miniaturized, low profile and cost-effective 3D packaging solutions.

## BARE DIE POP (BD-POP) EVALUATION

The BD-PoP bottom package (BD-PoPb) is typically an application processor or a baseband device with land pads placed on the top periphery of the package surface to enable the stacking of a mobile memory on the top of package (PoPt) as depicted above [4, 5]. The top package of PoPt contains memory devices stacked within and assembled, tested and yielded independently. The BD-PoPb and PoPt packages are usually stacked and assembled by reflowing process together on the application board to form the pre-stacked package-on-package (Z-interconnection with solder ball). A CuOSP or Ni/Au surface treatment process is utilized on the bottom pads of PoPb with lead-free ball options while Ni/Au on the top memory interface pads of PoPt is adopted. In order to enable the reduction of flip chip bump pitch, Cu pillar bump and BoL is usually utilized as compared to solder bump. For the same bump pitch of both bump types (Cu pillar bump and BoL as well as solder bump), a Cu pillar bump and BoL design created larger bump to bump spacing and resulted in more relaxed line and space design rule on substrate. In combination with elimination of solder-on-pad (SOP) and open solder resist design rules, these changes result in a lower cost package. The technology can also be used for conversion of wirebond designs into flip chip without the use of a redistribution layer (RDL), which would be a cost adder in bumping process. The BD-PoP provides the advantage of a denser design with larger die sizes and higher number of I/O counts within the same PoP package as compared to the wirebonded PoP version in the same body size and form factor. In addition, the use of fcPoP allows for potentially lower PoPb package height, thus reducing the total package stacked height post-SMT process. Improved device electrical performance can also be expected with the fcPoP package as with all other flip chip packages in comparison to wirebonded designs. A test vehicle with thin package profile and 15x15mm package size with 4-layer substrate and 200µm core thickness was evaluated. Die size is around 100mm<sup>2</sup> with 120µm die thickness. Package is with 0.4mm bottom solder ball pitch and utilized 0.2mm solder ball. Target maximum bottom package height is around 0.66mm. Fig. 1 illustrated the typical process flow for BD-PoPb. The warpage evaluation by using different underfill materials is shown in Fig. 2, which indicated that by using UF-A will cause nearly maximum 110µm warpage at high temperature (260°C) while by using underfill B will have better warpage performance, resulting in maximum warpage around 85µm at 260°C. However, this result still can't meet the warpage specification of 80µm at high temperature.

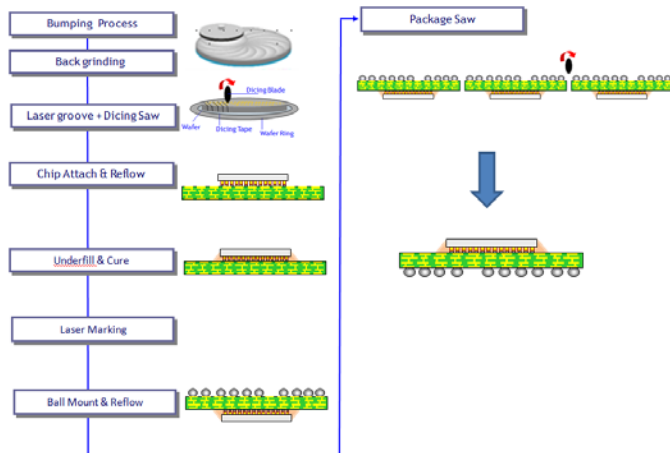


Fig. 1. Process flow of BD-PoP bottom package

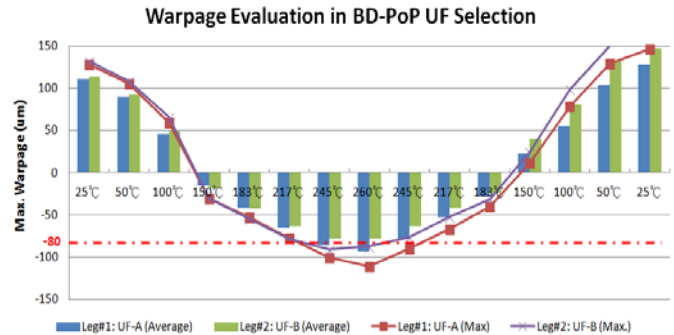
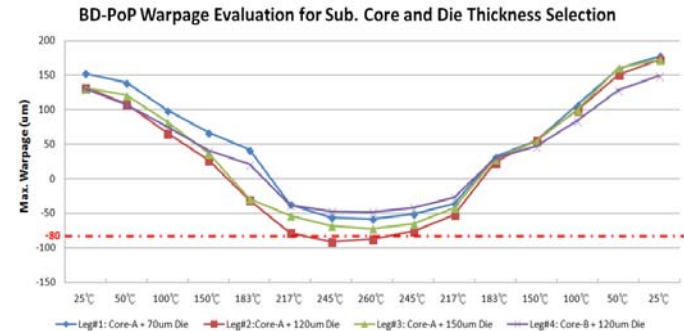


Fig. 2. Warpage behaviors in BD-PoP with 4L substrate and different underfill.

In order to improve the warpage behavior in BD-PoP, the combination of different substrate core material and die thickness was studied. Fig. 3 shows the warpage behavior study for different substrate core material as well as various die thickness of 70µm, 120 µm and 150 µm with the utilization of UF-B. From Fig. 3, it illustrates that using core-B and die thickness of 120µm will be the best combination to meet maximum warpage of 80µm at high temperature (260°C) specification. Fig. 4 shows the cross sectional image for this BD-PoP device, which indicated that the bottom package average height (BD-PoPb) is around 605µm and meets the maximum PoPb thickness target of 0.66mm.



Run #	Sub. Core	Die thickness	RT (25°C) Maximum	HT (260°C) Maximum
Leg# 1	Core-A	70µm	153	-58
Leg# 2	Core-A	120µm	132	-87
Leg# 3	Core-A	150µm	131	-72
Leg# 4	Core-B	120µm	130	-48

Fig. 3. Maximum warpage behaviors in BD-PoP with different die thickness and substrate core material.

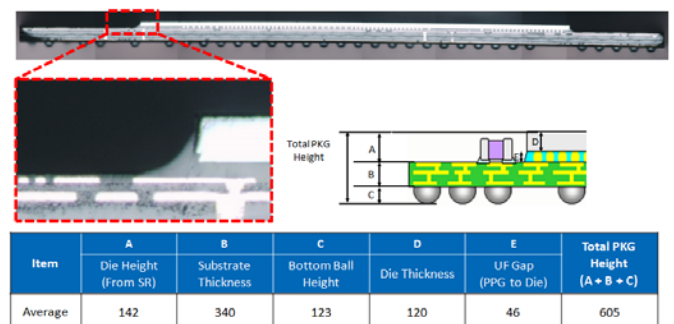


Fig. 4. Cross-sectional view in thin profile BD-PoPb

### MOLDED LASER POP (MLP-POP) EVALUATION

In order to drive aggressive package height reductions and finer mobile memory pitch down to 0.4mm and below, MLP-PoP was adopted as the ideal solution with its overmold configuration (OM MLP-PoP) and provides better warpage performance as compared to BD-PoP, especially at room temperature. The MLP-PoP stacks fully tested memory and logic packages to eliminate known good die (KGD) issues. It provides flexibility in mixing and matching IC technologies and enables assembly of larger dies in a thinner PoP stack up with top ball pitch finer than a bare die option. The surface treatment of CuOSP on the bottom substrate and top memory interface pads is typically utilized. It can support down to 0.3mm minimum ball pitch on bottom/BGA pads and much finer pitch on top memory interface pads of PoPb. Both capillary underfill (CUF) and molded underfill (MUF) are available in MLP-PoP but MUF technology allows for increased cavity size and larger die size with a lower assembly cost solution [6]. As MLP-PoP typically has the EMC material over the top surface of the die (overmold), the coplanarity and warpage improvement is been realized over BD-PoP is due to the use of overmold or mold cap. Mold shrinkage and other EMC material properties of modulus, coefficient of thermal expansion (CTE) and glass transition temperature (Tg), are modulators that can be optimized to provide a more flat package at room temperature and improved coplanarity. Thin package profile technologies for a maximum PoPb package thickness of 0.62mm with 1/2/1 4-layers BU substrate and 100 $\mu$ m core thickness as well as 15x15mm package size were studied. Die size was around 100mm<sup>2</sup> with 120 $\mu$ m die thickness. Mold thickness of 0.2mm was utilized. The package had a 0.4mm bottom solder ball pitch and utilized 0.2mm solder ball. Fig. 5 illustrated the typical process flow for MLP-PoP. The warpage evaluation by using different substrate core materials and EMC is shown in Fig. 6, which illustrated that Leg#2, #3 and #5 can meet maximum warpage of 80 $\mu$ m at high temperature. Among these three legs, EMC-C with substrate core A (Leg# 3) is the best solution to meet the coplanarity and warpage specification. Fig. 7 shows the cross sectional image for this MLP-PoP device, which indicated that the bottom package average height (MLP-PoPb) is around 565 $\mu$ m and achieved the maximum PoPb thickness target of 0.62mm. In addition, it showed the good solder joint through cross sectional inspection as well.

Fig. 5. Process flow of MLP-PoP bottom package with MUF

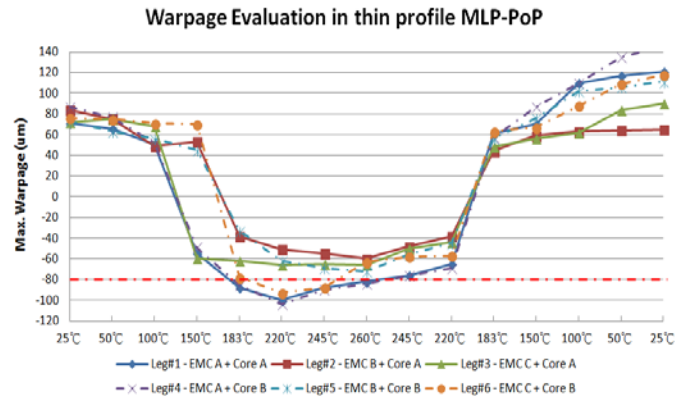


Fig. 6. Maximum warpage behaviors in MLP-PoP with 1/2/1 substrate (S/S:10ea in each leg)

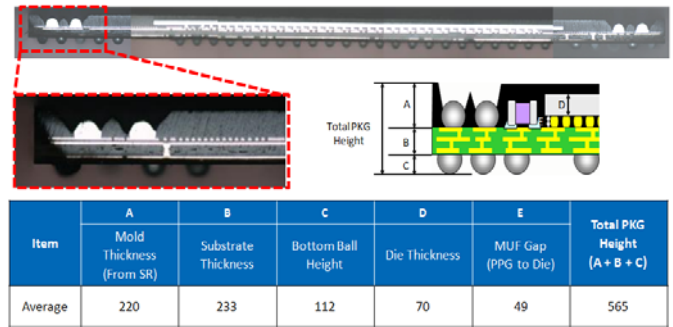


Fig. 7. Cross-sectional view in thin profile MLP-PoPb

Fig. 8 illustrated the X-ray inspection after chip attach process. It is clear that there was no abnormality on X-ray inspection process. Fig. 9 showed the C-Mode Scanning Acoustic Microscopy (C-SAM) and Through Scanning Acoustic Microscopy (T-SAM) result after MUF process, which indicated that there is no MUF void as well as delamination has been observed. This test vehicle also passed long term reliability test such as pre-condition of moisture sensitivity level (MSL3) as well as unbiased highly accelerated stress test (uHAST) of 192 hours, thermal cycling test condition B (TCB) of 1000 cycles and high temperature storage test (HTST) at 150 $^{\circ}$ C of 1000 hours without any defect observed. The package reliability results are illustrated in Fig. 10 by utilizing T-SAM inspection.

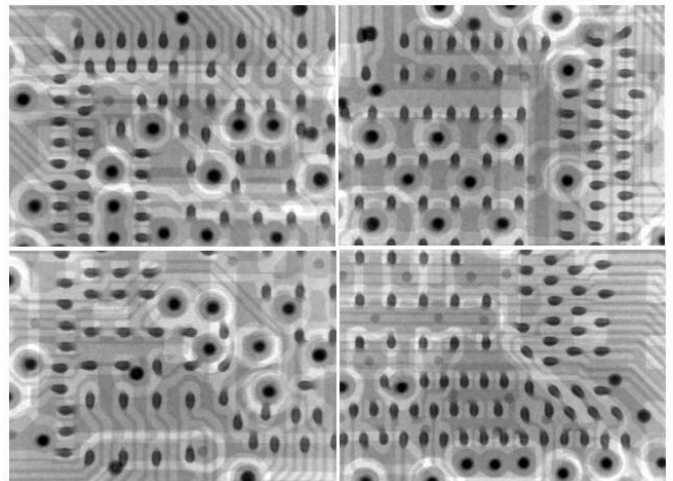
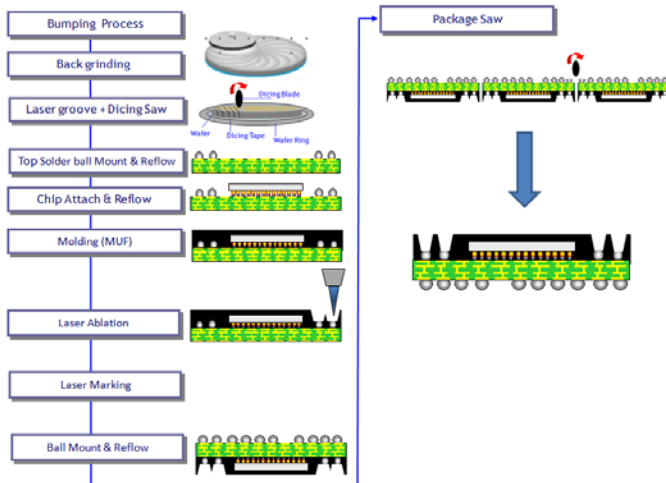


Fig. 8. X-Ray inspection after chip attach process

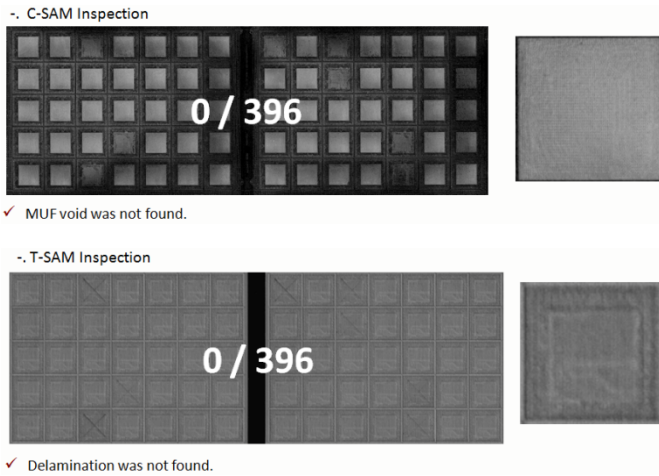


Fig. 9. C-SAM and T-SAM inspection after molding process

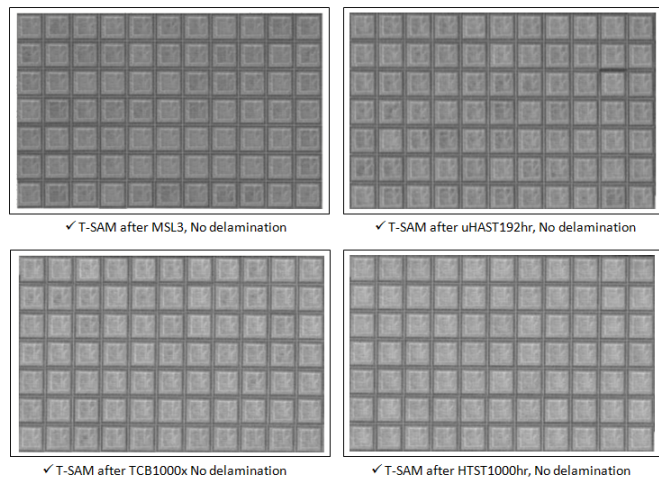


Fig. 10. Long term package reliability result in MLP-PoP

The pre-stack technology combines PoPb and PoPt packages into a single component as well as eliminate expensive yield loss at PCB-level SMT assembly stage. The pre-stack technology enables fine pitch PoPb to PoPt interconnection with associated higher pin counts, increased application processor and memory interface bandwidth, and thinner overall fcPoP height. Fig. 11 illustrated the pre-stack warpage behavior by utilizing different top mobile memory (memory - A and memory - B) with 0.45mm body thickness (substrate + molding), 0.5mm pitch and maximum PoPt height of 0.7mm. Through the warpage data, it not only demonstrated the capability of pre-stack process flow to stack the PoPt and PoPb in a single package, but also that it can have further warpage and coplanarity reduction.

Fig. 12 illustrated the total package cross-sectional image that package height is measured by ICOS inspection (consider warpage effect). The average total thickness was measured as 1.14mm, which met the required maximum total package height below of 1.2mm.

## CONCLUSIONS

This paper reports the evaluations of thin flip chip package-on-package (fcPoP) profile with bare die PoP (BD-PoP) and molded laser PoP (MLP-PoP) types. The study of different underfill, substrate core material as well as die thickness in BD-PoP for warpage behavior estimation was illustrated. The result also showed the BD-PoP structure can meet the warpage specification of 80µm and package maximum target thickness of 0.66mm (nominal thickness is 0.61mm). Meanwhile, the combinations of EMC and substrate core materials were evaluated not only to meet warpage criterion but also meet the low package profile target (max. is 0.62mm, nominal is 0.57mm). The long term reliability test with MSL3, uHAST192hr, TCB1000x and HTST1000hr were illustrated to show the good quality of this low profile MLP-PoP study. Moreover, by adopting pre-stacking technology, total package warpage and coplanarity behavior was demonstrated to have further improvement and meet maximum total package below 1.2mm requirement.

Leg #	Top memory	Mold Cavity	EMC	Max. Warpage @RT	Max. Warpage @HT
Leg#1	Memory - A	0.2mm	EMC - C	30µm	-47µm
Leg#2	Memory - B			38µm	-45µm

Warpage Evaluation after pre-stack

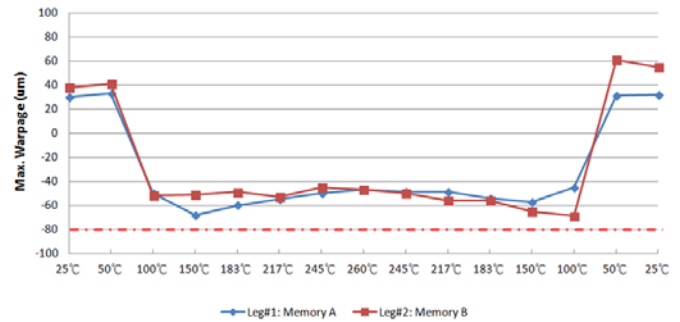
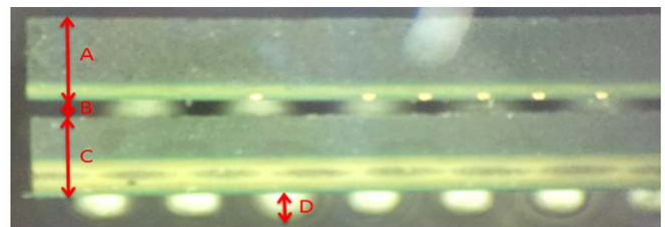


Fig. 11. Maximum warpage behavior in MLP-PoP after pre-stacking



Top package body thickness (A)	Gap (B)	Bottom package thickness (C)	Bottom ball stand-off height (D)	Total package height
0.46mm	0.11mm	0.45mm	0.12mm	1.14mm

Fig. 12. Cross-sectional view and thickness measurement in thin profile MLP-PoP after pre-stacking

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