Advanced Flip Chip Package on Package Technology for Mobile Applications

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Abstract*—With the rapid technology developments in the semiconductor industry, the mobile phone has evolved from a simple communication device to a complicated and highly integrated system with multiple functions and heterogeneous devices. Based on the fast growth in emerging markets for mobile applications, many wireless devices have jumped to 4G Long Term Evolution (LTE) communication platform and may ramp to 5G generation technology in the next two to three years. Moving forward with this trend, packaging semiconductor devices for mobile electronics is more challenging than ever before. As the demand of higher performance, higher bandwidth, lower power consumption and smaller form factor are increasingly required in portable mobile devices, standard flip chip packages such as fcCSP are not able to meet these requirements. Three-dimensional (3D) package-on-package solution with flip chip interconnect (fcPoP) has been widely utilized to successfully achieve these goals. With the ability to stack a logic processor and memory device in a single package, the utilization of fcPoP is becoming a preferred solution in the mobile market segment. It is well known that fcPoP technology developments are related to the evolution of mobile low power double data rate (LPDDR) memory, requiring lower voltage, lower power consumption and higher transition rates, a significant number of 4G LTE mobile devices are adopting fcPoP with LPDDR3 and are now migrating to LPDDR4 as well as finer silicon nodes (below 20nm). Challenges in finer pitch memory devices, thinner package profiles, stringent package warpage/coplanarity requirements and Surface Mount Technology (SMT) processes are successfully met with fcPoP technology. This paper reports the 3D package developments with flip chip technology, including bare die package-on-package (BD-PoP), molded laser package-on-package (MLP-PoP) as well as interposer package-on-package (I-PoP) to support high bandwidth or wide I/O memory. Various fcPoP vehicles have been designed and fabricated to demonstrate low profile (total package height less than 1.2mm) and much finer top ball pitch solutions for mobile applications. Package warpage/coplanarity control and reliability characterization are also illustrated. These results show fcPoP architecture is an enabling technology for highly integrated, miniaturized, low profile and cost-effective 3D packaging solutions

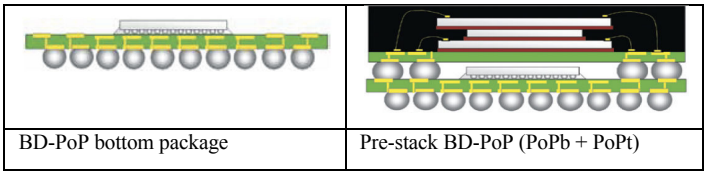
Keywords—Flip Chip, Bare Die Package-on-Package, Molded Laser Package-on-Package, MLP, Interposer PoP

I. INTRODUCTION

As the demands of higher performance, higher bandwidth, lower power consumption as well as multiple functions increases, the industry is driving advance technology developments in emerging markets, especially in portable and mobile devices to meet these requirements. The utilization of emerging technologies is pushing smaller form factor package designs with finer line width and spacing as well as improved electric and thermal performance and passive embedded technology capabilities. The communication platform in portable and mobile devices has also jumped from 2G to 3G and then to 4G LTE in past decade. Advanced silicon (Si) node (20nm and below) technology is another driving force in mobile applications to pursue the die size reduction, efficiency enhancement and lower power consumption in recent years. Based on these demands and evolution of the mobile communication platform, package types become more complicated and have migrated from wirebond packaging to flip chip interconnect when higher input/output (I/O) counts are needed [1, 2]. To meet the requirement of higher I/O counts, the flip chip chip scale package (fcCSP) has become the mainstream package type for mobile application processors (AP) as well as baseband processors (BB) [3]. Due to the fcCSP features, the mobile low power double data rate (LPDDR) memory is usually packaged in a side-by-side arrangement with AP/BB. For the purpose of having the shortest interconnection between these logic devices and LPDDR, 3D fcPoP has become a major package solution for achieving the best performance and efficiency as well as smaller form factor in a module/printed circuit board (PCB).

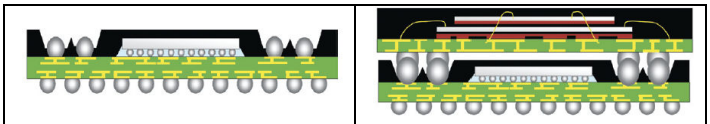
Since the industry adopted fcPoP as a dominant package approach to stack the logic processor and mobile memory in a single package for portable and mobile applications, the thin package profile of fcPoP has been widely discussed. Generally, for the purpose of bump pitch reduction and performance improvement, the need for Cu column design for flip chip bumps is required. Moreover, the adoption of Cu column and the associated Bond-on-Lead (BoL) technology provide substrate cost reduction through design rule relaxation, which is key for cost sensitive PoP packages and consumer electronics. The flip chip bare die package-on-package (BD-PoP) was introduced in 2008 and featured a flip chip bottom package configuration with Ni/Au pad surface treatment on the top substrate in order to stack with a mobile memory device

(shown in Fig. 1). Based on this structure, warpage and coplanarity is always the major issue to be overcome when driving thin package profiles in BD-PoP [4]. The top memory is usually with larger than 0.5mm ball pitch and limited memory I/O counts. Total package height (top memory + PoP bottom package) typically is above 1.3mm in BD-PoP applications. For the sake of driving thin package profiles as well as finer memory interconnection pitches, a new molded laser flip chip package-on-package (MLP-PoP) was introduced in mobile application processors in 2011. The MLP-PoP has epoxy molding compound (EMC) which covers the active die. The laser ablation process is used to expose the solder interconnect on the top substrate (see Fig. 2(a)). Another approach is named as expose die molded laser package-on-package (ED MLP-PoP), which utilizes film assist mold (FAM) technology to expose the active die top surface. The schematic is shown in Fig. 2(b). With these technologies, the warpage and coplanarity can be further reduced by suitable selection of EMC material and can support finer interconnection pitch of top mobile memory to 0.5mm and/or 0.4mm in volume production today. Maximum total package height of MLP-PoP can further reduced to 1.2mm and below.



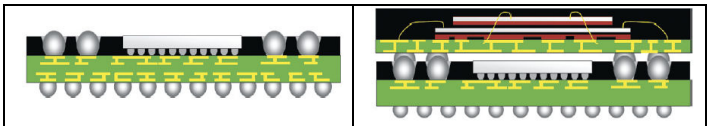
BD-PoP bottom package	Pre-stack BD-PoP (PoPb + PoPt)

Fig. 1. Schematic of bare die package-on-package (BD-PoP)



MLP-PoP bottom package	Pre-stack MLP-PoP (PoPb + PoPt)

(a)

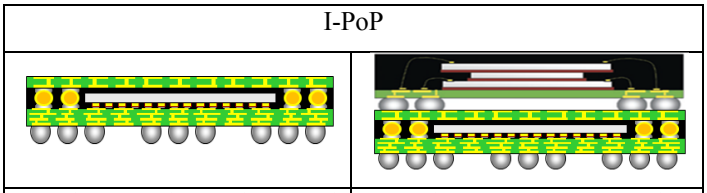


ED MLP-PoP bottom package	Pre-stack ED MLP-PoP(PoPb + PoPt)

(b)

Fig. 2 (a). Schematic of mold laser package-on-package (MLP-PoP; overmold); (b) Schematic of expose die mold laser package-on-package (ED MLP-PoP)

As more and more functions are designed in a chip to target the high-end mobile market, the die is becoming more than 10x10mm in size. With the bigger die size, it is challenging for the MLP-PoP structure to support top memory I/O counts of more than 300 I/O in a limited package size (14x14 or 15x15mm). In addition, memory packages with wide I/O counts (more than 500 I/O) is also expected to be the future trend in emerging market application. In order to solve the constraints of bigger die and package size limitations, top memory with wide I/O counts as well as customized mobile memory applications, the interposer package-on-package (I-PoP) technology is a strong solution. In comparison to the MLP-PoP structure, I-PoP has a top interposer substrate (a 2 layer substrate is typical) and the flip chip die is between the top interposer and bottom substrate. The peripheral interconnections between top interposer and bottom substrate can be made by copper column (CuC), copper cored solder ball (CCSB), solder ball, etc. Fig. 3 showed the schematic of I-PoP with CCSB configuration. The interconnection pitch on the bottom of the top interposer substrate can be smaller than mobile memory ball pitch to interconnect all mobile memory I/O counts. With the help of the top interposer substrate, the warpage and coplanarity can be further reduced as compared to MLP-PoP. The main challenge in I-PoP is how to drive maximum total package height to be less than 1.2mm and below. To satisfy future industry requirements for mobile applications, it is believed that fcPoP can provide versatile package structures to meet higher performance demands and will be the main package solutions for mid to high-end mobile devices.



I-PoP	
I-PoP bottom package with Cu cored solder ball (CCSB)	Pre-stack I-PoP with CCSB (PoPb + PoPt)

Fig. 3. Schematic of interposer package-on-package with Cu cored solder ball (I-PoP with CCSB)

II. Bare Die Package-on-Package (BD-PoP)

The BD-PoP bottom package (BD-PoPb) is typically an application processor or a baseband device with land pads placed on the top periphery of the package surface to enable the stacking of a mobile memory on the top of package (PoPt) as depicted above. The top package of PoPt contains memory devices stacked within and assembled, tested and yielded independently. The BD-PoPb and PoPt packages are usually stacked and assembled by reflowing process together on the application board to form the pre-stacked package-on-package (Z-interconnection with solder ball). A CuOSP or Ni/Au surface treatment process is utilized on bottom pads of PoPb with lead-free ball options while Ni/Au on top memory interface pads of PoPb is adopted. In order to enable the reduction of flip chip bump pitch, Cu column bump and BoL with is usually utilizes as compared to solder bump. For the same bump pitch of both bump types design (Cu column bump and BoL as well as solder bump), Cu column bump and BoL design created larger bump to bump spacing and resulted in more relaxed line and space design rule on substrate. In combination with elimination of solder-on-pad (SOP) and open solder resist design rules, these changes result in a lower cost package. The technology can also be used for conversion of wirebond designs into flip chip without the use of RDL, which would be a cost adder in bumping process. The process flow for BD-PoPb is illustrated in Fig. 4. The BD-PoP provides the advantage of a denser design with larger die sizes

and higher number of I/O counts within the same PoP package as compared to the wirebonded PoP version in the same body size and form factor. In addition, the use of fcPoP allows for potentially lower PoPb package height, thus reducing the total package stacked height post-SMT process. Improved device electrical performance can also be expected with the fcPoP package as with all other flip chip packages in comparison to wirebonded designs. A BD-PoP package offers the lowest cost package solution and with a memory interface pitch down to 0.4mm. Fig. 5 shows the warpage behavior in BD-PoP development with a 14x14mm package size and three to four layers in an embedded trace substrate (ETS) to drive thin package profile solutions. A 4L ETS with substrate thickness of 0.26mm as well as 3L ETS with substrate thickness of 0.24mm was evaluated. Through the warpage result, it showed that all evaluation results met a maximum warpage of 80um at high temperature (260℃) specification. The evaluation of Leg 2 of 3L ETS illustrated the better warpage behavior than others (Leg 2 and 3 are with different prepreg thickness). In addition, all three legs passed pre-condition of moisture sensitivity level (MSL2Aa and MSL3) as well as unbiased highly accelerated stress test (uHAST) of 192 hours, thermal cycling test condition B (TCB) of 1000 cycles and high temperature storage test (HTST) at 150℃ of 1000 hours without any defect observed.

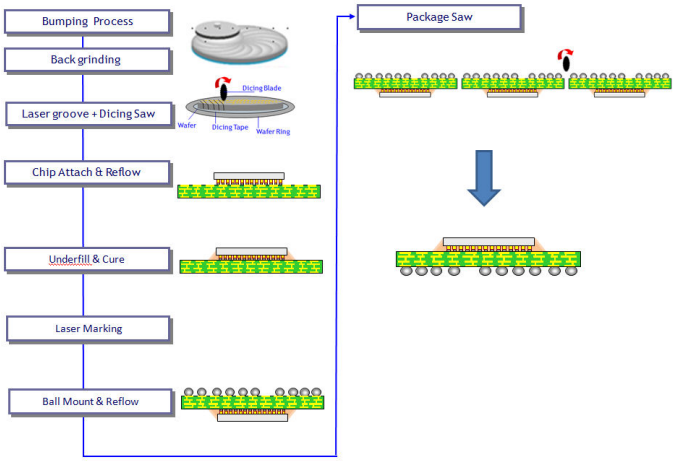


Fig. 4. Process flow of BD-PoP bottom package

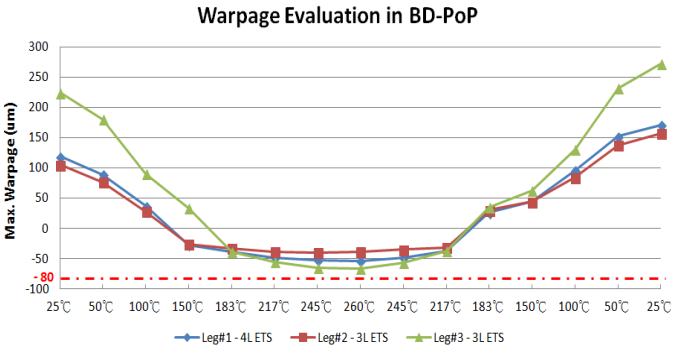


Fig. 5. Max. warpage behaviors in BD-PoP with 4L and 3L ETS (S/S: 10ea in each leg)

III. MOLDED LASER PACKAGE-ON-PACKAGE (MLP-POP)

As the BD-PoP is usually for applications with mobile memory interface pitch of 0.65mm or 0.50mm, finer pitch of 0.4mm was typically not considered feasible in BD-PoP due to the stack geometries and tight vertical clearances between PoPt and PoPb. In addition, the demand of thinner package heights cause challenges to meet package warpage and coplanarity specifications. In order to drive aggressive package height reductions and finer mobile memory pitch down to 0.4mm and below, MLP-PoP was adopted as the ideal solution with its overmold configuration (OM MLP-PoP) and provides better warpage performance as compared to BD-PoP, especially at room temperature. The MLP-PoP stacks fully tested memory and logic packages to eliminate known good die (KGD) issues. It provides flexibility in mixing and matching IC technologies and enables assembly of larger dies in a thinner PoP stack up with top ball pitch finer than bare die option. The surface treatment of CuOSP on the bottom substrate and top memory interface pads is typically utilized. It can support down to 0.3mm minimum ball pitch on bottom/BGA pads and much finer pitch on top memory interface pads of PoPb. Both capillary underfill (CUF) and molded underfill (MUF) are available in MLP-PoP but MUF technology allows for increased cavity size and larger die size with a lower assembly cost solution. The typical process flow for MLP-PoP bottom package with MUF is illustrated in Fig. 6.

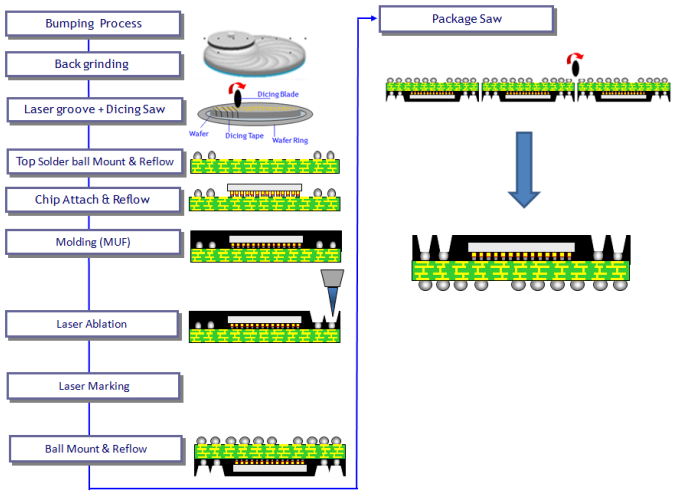


Fig. 6. Process flow of MLP-PoP bottom package with MUF

MLP-PoP allows for further height reduction and the use of a tight memory interface pitch down to 0.27mm currently. As MLP-PoP typically has the EMC material over the top surface of the die (overmold), the coplanarity and warpage improvement is been realized over BD-PoP is due to the use of overmold or mold cap. Mold shrinkage and other EMC material properties of modulus, coefficient of thermal expansion (CTE) and glass transition temperature (Tg), are modulators that can be optimized to provide a more flat package at room temperature and improved coplanarity efficiently. The presence of the EMC also allows for reduced

package height through implementation of film-assisted molding (FAM) that enables the exposed die solution in MLP-PoP (the next-generation of MLP-PoP). The technology of ED MLP-PoP results in further package height reduction compared to OM MLP-PoP and will enable maximum package heights less than 0.7mm (including warpage) [5]. Thin package profile technologies for a maximum PoPb package thickness of 0.62mm with 1/2/1 4-layers BU substrate as well as the exposed die solution (ED MLP-PoP) with a maximum 0.54mm PoPb package thickness was qualification. Fig. 7 shows the warpage behavior in OM MLP-PoP development with 15x15mm package size and maximum 0.62mm PoPb height that was qualified and passed pre-condition of MSL3, uHAST 192hr, TCB 1000x and HTST (150℃) 1000hr without any failure by using EMC-B. The corresponding PoPb cross-sectional view is illustrated in Fig. 8.

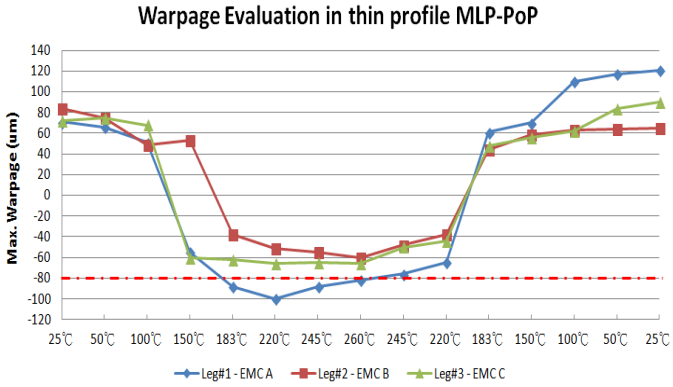


Fig. 7. Max. warpage behaviors in OM MLP-PoP with 1/2/1 substrate (S/S: 10ea in each leg)

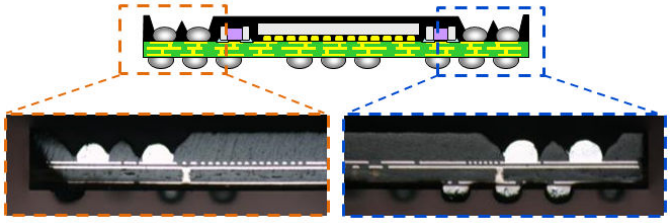


Fig. 8. Cross-sectional view in thin profile OM MLP-PoP

Fig. 9 illustrates the ED MLP-PoP development status for top memory interface pitch as 0.27mm. The package size is 14x14mm with around 10x10mm die size and utilized a 1/2/1 4-layers substrate. The long-term reliability test was passed and feasibility validated to support the finer mobile memory ball pitch down to 0.27mm by pre-stack technology. In Fig. 10, it was demonstrated that the capability of pre-stack process flow to stack the PoPt and PoPb in a single package.

The pre-stack technology combines PoPb and PoPt packages into a single component as well as eliminate expensive yield loss at PCB-level SMT assembly stage. The pre-stack technology enables fine pitch PoPb to PoPt interconnection with associated higher pin counts, increased application processor and memory interface bandwidth, and thinner overall fcPoP height. SCL leads the industry in development and implementation of this key technology, driving the pre-stack capability down to 0.2mm top ball pitch (TBP). The 0.2mm TBP was qualified with fan-out wafer level package technology in a PoP configuration called eWLB-PoP (Embedded Wafer Level Ball Grid Array Package-on-Package).

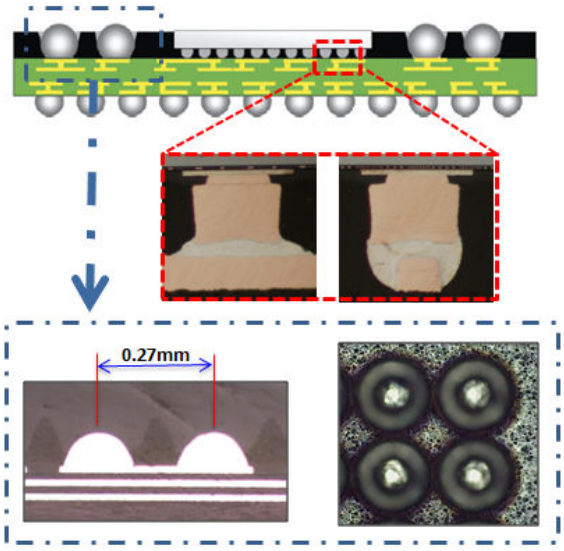


Fig. 9. Cross-sectional view for 0.27mm top ball pitch in ED MLP-PoP

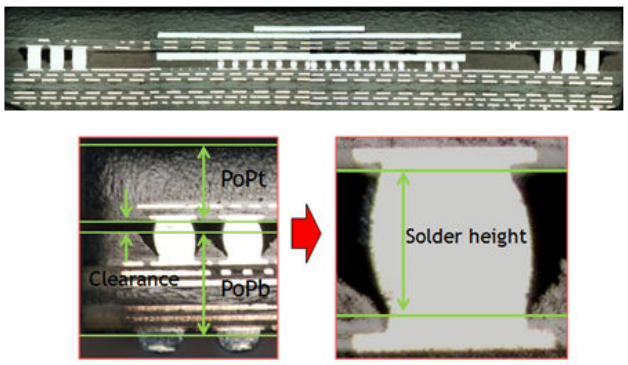


Fig. 10. Pre-stack result in ED MP-PoP with 0.27mm top ball pitch

IV. Interposer Package-on-Package (I-PoP)

The continued demands for higher level integration has led the industry to evaluate new fcPoP technologies and propose to be utilized with stacking of wide I/O counts and/or next generation mobile memory. The interposer package-on-package (I-PoP) is one of the new technology solutions to achieve these goals, features a top interposer substrate that interconnects the top mobile memory and bottom package peripherally by using copper column (CuC), copper cored solder ball (CCSB), solder ball, etc. The top interposer substrate can be designed in a different top and bottom ball pitch to connect top mobile memory and bottom package, respectively. With the I-PoP structure, die size limitations can

be overcome by using finer interconnection pitch (or called PoPb TBP), providing the flexibility to allow any memory interface pitch application. Moreover, with the help of top interposer substrate, package warpage and coplanarity can be further improved as compared to MLP-PoPb package because the I-PoP total stiffness is enhanced with the addition of the top interposer substrate. The cross-sectional views of I-PoP with CCSB interconnection are illustrated in Fig. 12.

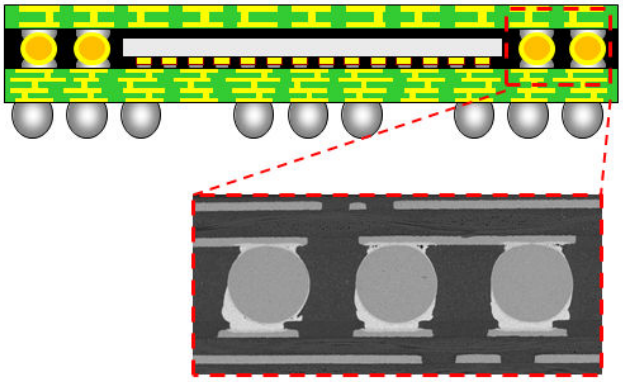


Fig. 12. Cross-sectional view for I-PoP with Cu cored solder ball (CCSB) interconnections.

Thin profile I-PoP is an important topic in the industry as it added a top interposer substrate increasing PoPb package height. However, due to the benefit of total stiffness enhancement with the use of top interposer substrate, a thinner bottom substrate can be utilized to compensate the package height increment. Even though the thinner bottom substrate adoption may result in larger warpage and coplanarity, it can be compensated with the use of top interposer substrate. Based on SCL's experience, the maximum I-PoP bottom package height of 0.69mm (nominal thickness as 0.64mm) with a 15x15mm package and a 1/2/1 4-layers bottom substrate was qualified without any negative impact to MSL3 pre-condition, uHAST96hr, TCB1000x and HTST1000hr. The interconnection pitch (top ball pitch) between the top interposer and bottom substrate was also qualified down to 0.25mm.

Fig. 13 illustrates the package level reliability result of MSL3, TCB1000x, uHAST192hr and HTST1000hr in a 15x15mm I-PoP with 0.35mm TBP of CCSB interconnections, which clearly shows that there is no interconnection damage occurred through these cross-sectional views. The corresponding maximum warpage behavior is illustrated in Fig. 14, which showed the maximum warpage value was well controlled to be less than 40μm at high temperature and meet the specification (maximum of 80μm at high temperature in usual).

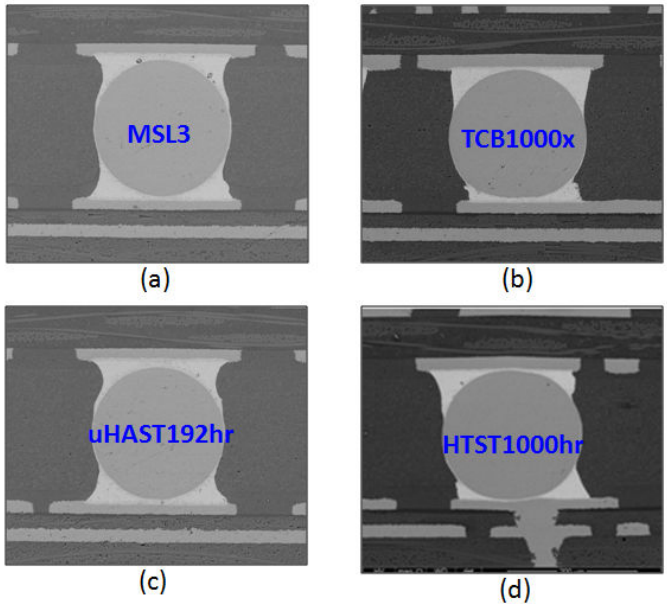


Fig. 13. Package level reliability result in I-PoP with CCSB interconnections.

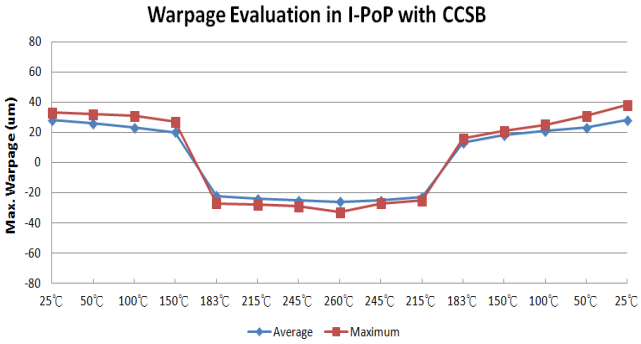


Fig. 14. Average and maximum warpage behaviors in I-PoP with CCSB interconnections (S/S: 10ea in each leg)

CONCLUSIONS

This paper reports various flip chip package-on-package (fcPoP) solutions in the current and emerging market for portable and mobile applications. The fcPoP technologies includes BD-PoP, MLP-PoP and I-PoP as well as their related structures, development status, warpage distribution and package reliability test result were discussed. If the top mobile memory ball pitch (TBP) is larger than 0.4mm, the BD-PoP may be a good candidate for a package solution. When fcPoP TBP becomes finer, MLP-PoP will be the best solution to support finer TBP less than 0.4mm. In addition, if wide I/O counts and large die size is needed in a package, I-PoP will be a strong package solution. With the rapid technology developments in the semiconductor industry to drive higher performance, higher bandwidth, lower power consumption and multiple functions on mobile application, it is believed that fcPoP architecture is a cost-effective 3D packaging solutions for highly integrated, miniaturized and low profile enabling technology.

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