“Design and Stress Analysis for Fine Pitch Flip Chip Packages with Copper Column Interconnects”

by

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***Abstract*—As the demand for high input/output (I/O) density, package miniaturization, high frequency operation and better thermal, mechanical and electric performance increases, flip chip packaging technology is rapidly growing as a solution to successfully achieve these goals. With handheld electronic devices, hot consumer products, graphics cards and memory packages in high demand, fine pitch flip chip packages (fcFBGAs) with bond-on-lead (BOL) interconnection are increasingly being pursued and widely studied in the electronic industry. BOL technology uses copper (Cu) column bumps that attach to narrow pads or traces without any solder resist confinement (open solder resist (SR)) in the peripheral I/O region of the die as opposed to a conventional circular bond-on-capture pad (BOC) structure. The BOL interconnection enables significantly higher routing densities at a lower cost for a given set of design rules. Although the advanced BOL packaging structure has been proven to have high stress resistance in extremely low-k (ELK) layers which prevents damage in finer silicon nodes, the increased risk of Cu trace peeling and/or Aluminum (Al) pad/under bump metallization (UBM) layer delamination can be caused by excess stresses. It is important to study these failure phenomena in 28-nm ELK fcFBGA with copper column interconnects. For the purpose of validating possible failure types in the 28-nm ELK fcFBGA with Cu column BOL interconnects, the three-dimensional finite element analysis (FEA) was adopted. The stress responses for each of the components were also obtained to determine the critical area that may potentially result in failures in this structure. Furthermore, to reduce the critical stress and enhance the reliability in a 28-nm ELK fcFBGA with Cu column BOL interconnects, a parametric discussion that captures the most significant factors impacting the stresses was studied. The result of this study provides a superior design for stress reduction to lower the risks of Cu trace peeling, Al pad/UBM delamination and ELK damage. Through this study, FEA simulations and corresponding validations can help to prevent the critical failure issues that are impacted by improper material and geometry designs in 28-nm ELK fcFBGA with Cu column BOL interconnects.**

Keywords—Fine pitch flip chip packages, bond-on-lead, bond-on-capture pad, finite element analysis, Cu column bump, mechanical simulation

I. INTRODUCTION

Flip chip packages are now widely used in the semiconductor industry for applications such as handheld electronic devices, smartphones, tablets, ASICs, PC chipsets, graphics, network and communication packages, etc. Due to the advantages of high I/O density, package miniaturization, better thermal and electric performance and high frequency operation, the flip chip package becomes a strong packaging solution to achieve these goals. Even though flip chip is not typically considered a low cost package, the increasing economies of scale for flip chip production volume in the industry (estimated to be 24 billion units in 2016) considerably reduce the cost impact [1]. According to the investigation of Yole Developpment, the total flip chip market value will reach $20B in 2015 and is expected to grow aggressively [1].

The conventional flip chip package utilized eutectic solder bump for the interconnections between the die and substrate. Due to the "Restriction of the use of certain hazardous substances" (RoHS) policy, the eutectic solder bump is being replaced by lead-free solder bump. However, with lead-free (LF) solder bump, the bump pitch is typically limited to 150μm and is very challenging to achieve bump pitches less than 120μm. As the bump pitch decreases, the risks of electrical shorts due to bump bridging and limited spacing for signal routing increase. To overcome these risks and achieve a finer pitch interconnection, Cu columns are employed. By utilizing Cu column, bump pitches can be reduced to 120μm and below. Moreover, since Cu column is more rigid than LF solder, the risk of bump bridging between adjacent bumps can be reduced. A larger spacing for signal routing can be achieved as well. There are two different interconnection types which are used for Cu column. One is bond-on-capture pad (BOC) interconnection and the other is BOL interconnection [2, 3], as illustrated in Fig. 1. BOC technology utilizes Cu column with pre-solder bumps attached to a Cu pad on the substrate (solder on pad or SOP) and a solder resist opening (SRO) on the Cu pad while the BOL technology uses Cu column (usually in circular or octagonal shapes) that attach to a narrow trace without any solder resist confinement in the peripheral I/O region of the die (with open SR). Because the components are more rigidly bonded together in the BOC structure, it will cause increased stress in ELK layers, UBM and bump configurations due to the coefficient of thermal expansion (CTE) mismatch between the die and substrate as compared to the BOL structure [4]. In order to prevent ELK damage, the use of Cu column BOL interconnection has been proven to have high stress resistance in ELK layers in finer silicon nodes [5-7]. However, the potential risk of Cu trace peeling and/or Al pad/UBM layer delamination caused by excess stress may occur. In addition, the Cu column BOL approach not only

significantly increases the routing efficiency and I/O density in the top most layer of the package but also reduces the cost of flip chip packages by utilizing 2, 3 or 4 layer substrates for cost reduction. For the purpose of having an efficient signal routing of the design layout, the Cu column is utilized in flip chip package as well. Hence, it is important to study the failure phenomena in 28-nm ELK fcFBGA with Cu column BOL interconnects.

In order to determine the critical area that may potentially result in failures and validate possible failure types in the 28-nm ELK fcFBGA with Cu column BOL interconnects, the three-dimensional finite element analysis (FEA) was utilized. Since the electronic packaging material properties and geometrical dimensions are well known to have significant effects on mechanical behaviors in packages, a parametric discussion includes three factors: 1) die (die size and thickness, Al pad size and thickness, UBM and PI opening size, PI thickness); 2) bumps (Cu bump, Ni, lead free solder height and bump orientation); and 3) substrates (substrate layer, Cu trace width and thickness). In addition, the effects on PI existence were studied and the most significant factors that influence the stresses were captured. A number of superior designs for stress reduction to lower the risks of Cu trace peeling, Al pad/UBM delamination and ELK damage were developed as well. The results of FEA simulations and corresponding validations will be helpful in reducing the critical stress that is caused by improper material, geometry selection and preventing the potential failure risks in 28-nm ELK fcFBGA with oblong Cu column BOL interconnects.

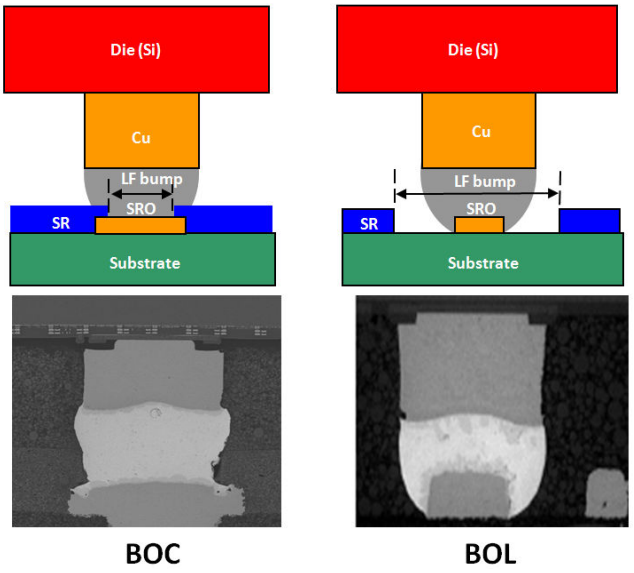


Fig. 1. Schematics and cross-sectional images of BOC and BOL structure.

II. FINITE ELEMENT MODELING ANALYSIS

For the sake of analyzing the mechanical behaviors of fcFBGA with oblong Cu column BOL interconnects, the test vehicle with a 6x6mm^2 die size in a 12x12mm^2 package body was utilized. The die thickness of 150µm high and a two-layer build-up substrate with the total thickness of 170µm was employed (core thickness was 100µm). The 5µm thick polyimide with a corresponding opening of 65x30µm and a 1.9µm thick passivation layer (SiN with USG) with corresponding opening of 75x50µm was designed. The UBM size was 95x50µm and metal pad on die side was approximately 99x75µm. The LF solder was attached to a narrow Cu trace of 25µm wide and 17µm height without any solder resist confinement in the peripheral I/O region of the die. The bump structure composition was Cu/Ni/SnAg material and the thickness was 30/3/25µm. The finite element model and the applied boundary condition for a 28-nm ELK fcFBGA with Cu column BOL interconnects is illustrated in Fig. 2 (due to symmetry, only a quarter model is presented). The employed material properties are listed in Table I, where *E*, ν, CTE and Tg are Young's modulus, Poisson's ratio, coefficient of thermal expansion and glass transition temperature, respectively.

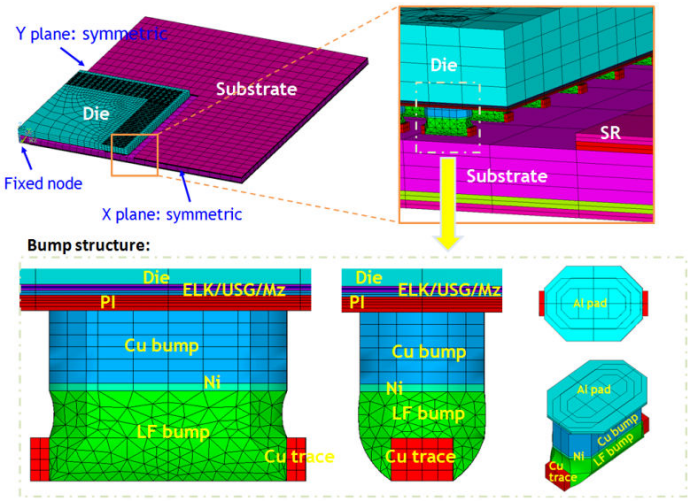


Fig. 2. Finite element models and applied boundary conditions.

Table I. Material properties in fcFBGA with Cu column BOL interconnects.

Material	E (GPa)	ν	CTE (ppm/˚C)
Die	131	0.28	2.8
ELK	10	0.2	6.5
USG	66	0.18	0.57
Mz (metal)	110	0.34	17
PI (Polyimide)	3.5	0.25	35
Passivation	137.5	0.206	1.907
Cu trace	110	0.34	17
Solder resistant (SR)	3.2	0.4	58/153 (Tg=105˚C)
LF (Sn96.5Ag3.5) [8]-[10]	56.824 @ -65˚C 54.350 @ -25˚C 50.993 @25˚C 47.342 @ 75˚C 43.398 @ 125˚C	0.4	20.525 @ -65˚C 21.340 @ -25˚C 22.360 @25˚C 23.380 @ 75˚C 24.399 @ 125˚C
Substrate core	25 @ 25˚C 23.86 @ 150˚C 15 @270˚C	0.3	(10,10,24)/(6,6,158) (Tg=230˚C)
Cu column/UBM	110	0.34	17
Al pad	69	0.35	23.1

Fig. 3 illustrates the possible failure in 28-nm ELK fcFBGA with Cu column BOL interconnects by utilizing a scanning electron microscope (SEM). These failures were observed to

occur during the chip attach process. From Fig. 3, it was observed that the failure initially occurred at the corner of the Al pad and UBM layer and then caused the interface delamination between Al pad and UBM layer (Fig. 3(a)). Another failure was the Cu trace initially peeling near the corner of the Cu trace and substrate which then induced the interface delamination between the Cu trace and substrate (Fig. 3(b)).

Fig. 4 shows the simulation result when the loading condition went from 260°C to 25°C and the stress free condition of 260°C was applied to the model. From Fig. 4, it was found that the maximum stress occurred at the Al pad adjacent to UBM layer, which was possibly inducing the failure of Al pad/UBM delamination. In addition, a larger stress in Cu trace was also observed and may cause the risk of Cu trace peeling phenomenon in the package. The maximum principal stress in ELK layer was found to be located on the outermost bump structure. Fig. 5 illustrates the stress vector plot of Al pad/UBM layer as well as Cu trace/substrate and indicates the possible crack propagation direction by the excess induced stress. From Fig. 5, it was observed that the possible crack propagation direction was along the interface between Al pad and UBM layer as well as the interface between Cu trace and substrate. Thus, the failure was initiated at the corner of Al pad and UBM layer as well as at the edge of Cu trace to cause the delamination in fcFBGA with Cu column BOL interconnects. This was well aligned with the SEM results that are shown in Fig. 3.

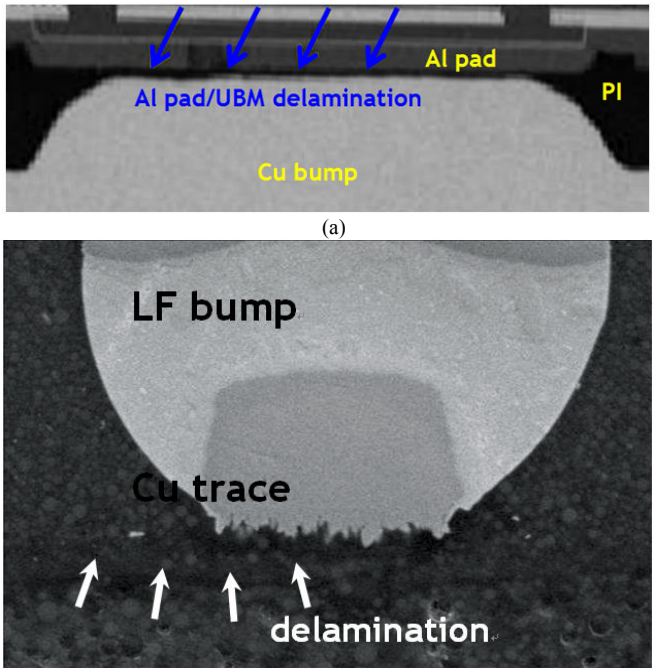


Fig. 3. Failure mode of (a) Al pad/UBM delamination; (b) Cu trace peeling.

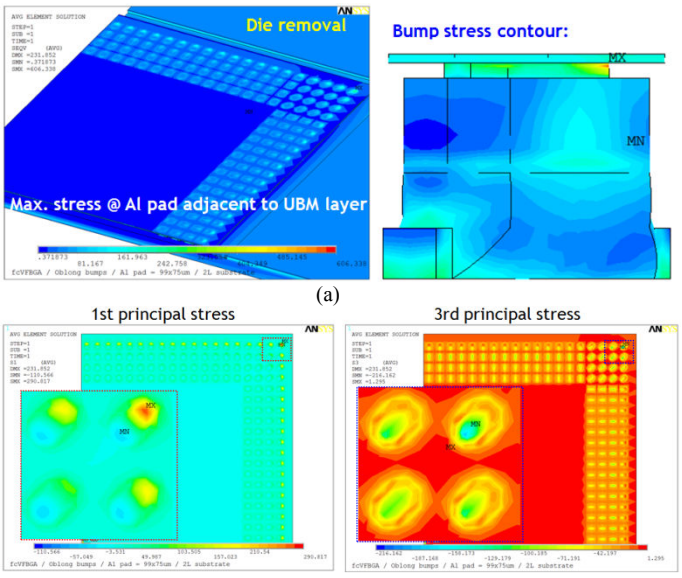


Fig. 4. Stress contour in fcFBGA with oblong Cu column BOL interconnects (a) von Mises stress contour; (b) principal stress contour in ELK layer.

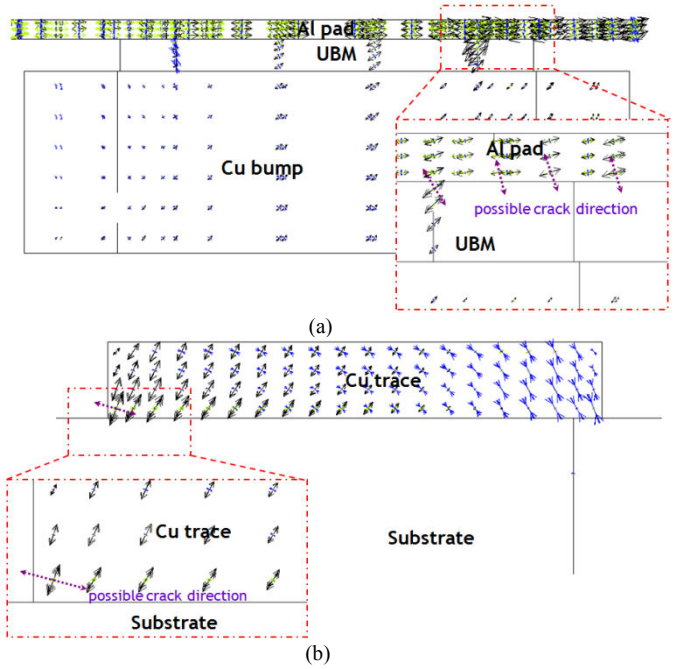


Fig. 5. Principal stress vector plot (a) near the Al pad and UBM layer; (b) near the Cu trace and substrate layer.

III. PARAMETRIC DISCUSSIONS

It is well known that electronic packaging material properties and geometrical dimensions play important roles in impacting the mechanical behaviors of a package. A number of failure phenomena come from utilizing the inappropriate geometry and/or mismatched materials. Inducing critical stresses during assembly processes which have been widely investigated in flip chip packages [11-14]. For the purpose of adopting compatible geometry and suitable materials in fcFBGA to prevent the potential failure risks, studying design

reliability is important. With the assistance of FEA, the parametric simulations for fcFBGA with Cu column BOL interconnects were studied to understand the essential effects of geometry and material properties that affect the mechanical behaviors, especially for the stress responses in ELK layer, Al pad/UBM layer and Cu trace. The material properties of the baseline model are shown in Table I and the parameters and ranges examined are listed in Table II. The loading condition was set to be from 260°C to 25°C.

Through the parametric review with FEA, the three levels parametric analysis was utilized to study the impact of significant factors on the stress responses of ELK, Al pad/UBM and Cu trace in fcFBGA with Cu column BOL interconnects. The simulation results are illustrated in Table III-V. Table III lists the significant factor to impact the stress in ELK layer, which shows the die thickness is the key factor and the Al pad size thickness as well as PI opening size significantly affects ELK stress as well. It was found that the effect of die thickness is proportional to the ELK stress while Al pad size, thickness and PI opening size is inversely proportional to the ELK stress. Hence, it is recommended to have thinner die or a larger PI opening size as well as larger and thicker Al pad to prevent the risk of ELK layer damage. Moreover, it is observed that 2-layer substrate layout will have smaller ELK stress due to the fact that 2-layer substrate is more compliant and flexible than 4-layer substrate to reduce the stress.

Table II. Selected parameters list in parametric simulations.

	Parameters	Range
Die	Al pad size	99x54,99x75,99x99 (μm)
	Al pad thickness	1,3,5 (μm)
	Die thickness	100,150,200 (μm)
	UBM size	95x40,95x45,95x50 (μm)
	PI opening size	65x20,65x30,65x40 (μm)
	PI thickness	3,5,7 (μm)
Bump	Cu bump height	20,30,40 (μm)
	Ni thickness	1,3,5 (μm)
	LF bump height	10,20,30 (μm)
Substrate	Substrate layout	2L,3L,4L
	Cu trace thickness	14,17,20 (μm)
	Cu trace width	20,25,30 (μm)

Table III. Significant factors to impact the ELK stress

➢ Top significant factors to ELK stress:

Significant factor		Level	Impact	Ranking
Die	Al pad size	99x54,99x75,99x99 (μm)	+6.5%/-4.2%	4 (10.7%)
	Al pad thickness	1,3,5 (μm)	+17.4%/-6.6%	2 (24.0%)
	Die thickness	100,150,200 (μm)	-35.2%/+48.6%	1 (83.8%)
	PI opening	65x20,65x30,65x40 (μm)	+7.2%/-13.4%	3 (20.6%)
Substrate	SBT layout	2L,3L,4L	-4.9%/+5.2%	5 (10.1%)

Table IV shows the parametric result for the stress in Al pad/UBM layer, which indicates the substrate layout design, Al pad thickness and PI opening size are key factors. The stress in Al pad/UBM layer was also impacted by changing PI thickness, bump height, die thickness and Al pad size. To reduce the stress in Al pad/UBM layer and avoid the associated delamination risk, a better solution uses 2-layer substrate or increasing Al pad thickness (from 3μm to 5μm) as well as enlarging PI thickness (from 5μm to 7μm). Table V illustrates the significant factors to affect the stress in Cu trace. It was found that the critical factor to have lower Cu trace stress is utilizing 2-layer substrate instead of a 3-layer or 4-layer substrate. The reason comes from that fact that Cu traces are electroplated on the substrate and substrates with few layers possess a higher compliant tolerance to the stress. In addition, it was also observed that adopting a larger Cu trace width and smaller Cu trace thickness was a good method to reduce the Cu trace stress. Hence a substrate layout with few layers is recommended for releasing the Cu trace stress response (but higher warpage will be induced) and a wider/thinner Cu trace design is helpful as well.

Table IV. Significant factors to impact the Al pad/UBM stress

➢ Top significant factors to Al pad/UBM stress:

Significant factor		Level	Impact	Ranking
Die	Al pad size	99x54,99x75,99x99 (μm)	+6.6%/-3.4%	7 (10.0%)
	Al pad thickness	1,3,5 (μm)	+13.4%/-13.2%	2 (26.6%)
	Die thickness	100,150,200 (μm)	-2.6%/+8.1%	6 (10.7%)
	PI opening	65x20,65x30,65x40 (μm)	+17.9%/-3.2%	3 (21.1%)
	PI thickness	3,5,7 (μm)	+3.8%/-9.9%	4 (13.7%)
Bump	LF bump height	10,20,30 (μm)	+7.1%/-4.0%	5 (11.1%)
Substrate	SBT layout	2L,3L,4L	-13.4%/+24.1%	1 (35.5%)

Table V. Significant factors to impact the Cu trace stress

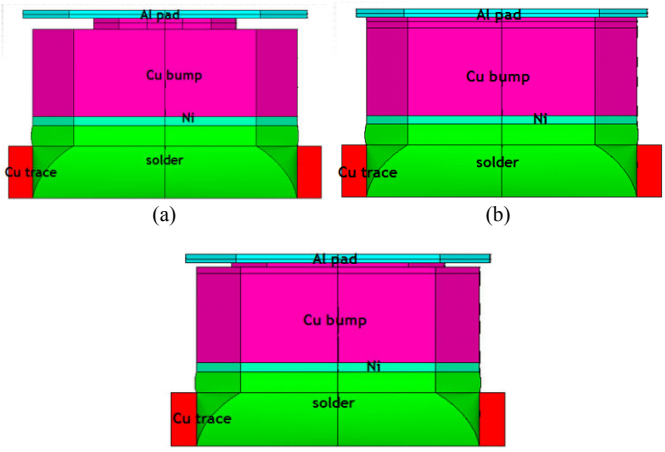
➢ Top significant factors to Cu trace stress:

Significant factor		Level	Impact	Ranking
Substrate	SBT layout	2L,3L,4L	-35.6%/+68.7%	1 (104.3%)
	Cu trace thickness	14,17,20 (μm)	-3.7%/+6.5%	3 (10.2%)
	Cu trace width	20,25,30 (μm)	+6.1%/-4.4%	2 (10.5%)

IV. Effect on PI Layer Existence

For the purpose of pursuing low cost flip chip packages, the non-PI structure was recently studied. In this structure, the Cu column is electroplated on the Al pad/passivation layer without any process of PI layer coating. The cost saving will be around $30 per wafer as compared to conventional PI Cu column bumping processes. The schematics of PI Cu column BOL, non-PI Cu column BOL without UBM overlap on the top passivation layer (i.e., the UBM size is less than passivation opening size) and non-PI Cu column BOL with UBM overlap on the top passivation layer (i.e., the UBM size is larger than passivation opening size) are illustrated in Fig. 6., respectively (with the same UBM size). Fig. 7 illustrates the stress contours in Al pad/Cu bump and indicates the maximum stress that occurs at the Al pad if the UBM size is less than the passivation opening size while located on Cu bump (UBM) if the UBM size is larger than the passivation opening size in non-PI Cu column BOL devices. The stress comparison in Cu bump, Al pad and ELK layer is shown in Fig. 8. It was found that smaller stress responses resulted in PI Cu column BOL devices. Much larger stress in Cu bump and Al pad was observed in the non-PI Cu column BOL device and became worse if the UBM size was less than the passivation opening size that was employed. The Cu bump and Al pad stress in the non-PI structure with a larger passivation opening size is

almost 60% and twice larger than in the conventional PI structure, respectively. Around a 30% Al pad stress increment was found in the non-PI structure with a larger passivation opening size as compared to the non-PI structure with a smaller passivation opening size. The reason comes from the fact that Cu columns directly attach to Al pad without any contact with passivation and PI layer to release the corresponding stress in this case. In addition, a larger ELK stress occurred if the UBM size is smaller than the passivation opening size as compared to if the UBM size is larger than the passivation opening size. There is a 10% gap between both cases, therefore, through this comparison, a larger UBM size and smaller passivation opening size is recommended to avoid the ELK damage.



- Fig. (a)-(c) are with the same UBM size.

Fig. 6. Schematics of Cu column BOL interconnects (a) PI structure; (b) non-PI structure and without UBM overlap on the passivation layer; (c) non-PI structure and with UBM overlap on the passivation layer.

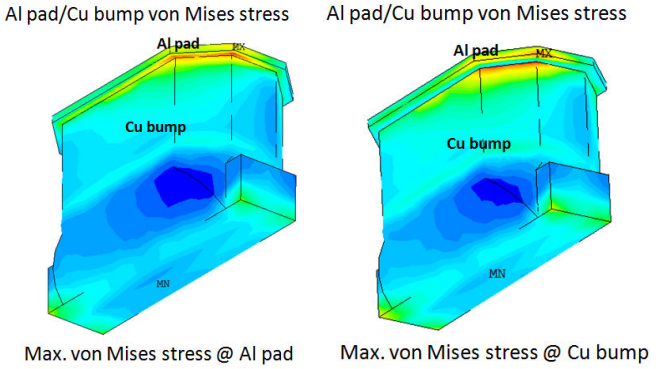


Fig. 7. Stress contours of non-PI oblong Cu column BOL interconnect (a) structure without UBM overlap on the top passivation layer; (b) structure with UBM overlap on the passivation layer.

V. CONCLUSIONS

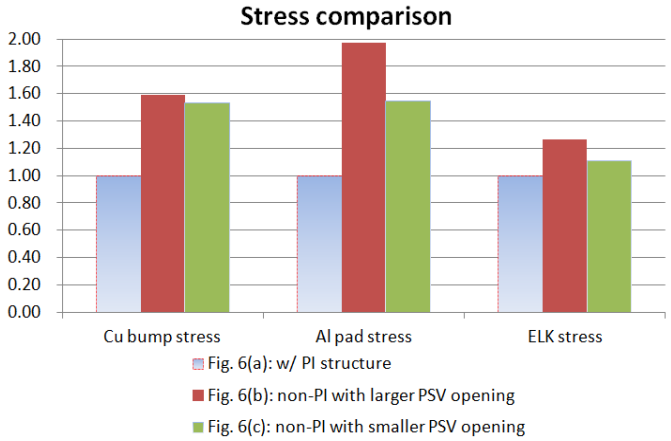
The mechanical behaviors in fcFBGA with Cu column BOL interconnects have been studied by the FEA modeling in this paper. The critical stress in the interface of Al pad/UBM layer as well as Cu trace/substrate was observed and these places may induce the potential risks of Al pad/UBM delamination or Cu trace peeling, which aligned with reliability failure results that have been investigated. For the purpose of capturing the most significant factors and the corresponding impact levels of these factors to ELK, Al pad/UBM and Cu trace stress responses in fcFBGA with Cu column BOL interconnects, parametric simulation studies were illustrated. The comparison of the effect on PI layer existence was discussed as well. The presented results can be valuable design guidelines when the adequate design for stress reduction in fcFBGA with Cu column BOL interconnects is required. Some important results and recommendations for stress reduction are summarized as follows:

(1) A thinner die or a larger PI opening size as well as a larger and thicker Al pad is useful to prevent the risk of ELK layer damage.

(2) By utilizing the reduced substrate layer layout design or increasing Al pad thickness and PI thickness can avoid the risk of Al pad/UBM delamination.

(3) Fewer substrate layers in a layout design and a wider/thinner Cu trace design is recommended for releasing Cu trace stress.

(4) For a non-PI Cu column BOL structure, greater stress in the Al pad, Cu bump (UBM) and ELK dielectric layer was observed. A larger UBM size and smaller passivation opening size are recommended to avoid the ELK damage in the non-PI Cu column BOL structure.



- Stresses for with PI structure in Fig. 6(a) are normalized as 1.

Fig. 8. Stress comparison of with PI and non-PI Cu column BOL devices.

ACKNOWLEDGMENT

The authors would like to thank L. Lavin at STATS ChipPAC Inc., USA for editing this paper.

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