“Electromigration for Advanced Cu Interconnect and the Challenges with Reduced Pitch Bumps”

by

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Electromigration for Advanced Cu Interconnect and the Challenges with Reduced Pitch Bumps

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Abstract

Cu Column bump has seen growing adoption in both high–end and low-cost mobile devices as well as in consumer, computing and networking devices. Higher input/output (I/O) density and very fine pitch requirements are driving very small feature sizes such as small bump on a narrow pad or bump on lead (BOL), while higher performance requirements are driving increased current densities, thus making electromigration (EM) performance a real and serious concern.

As the fine pitch and bump sizes decrease (in both mass reflow and thermo compression bonding processes) and the current density through the bump increases, EM reliability is becoming an alarming issue across the industry. High current density in Cu column bump combined with Joule heating may easily cause an early EM failure in field applications. Many researchers [1-3, 11-13] have published copper column EM data with a number of studies and EM variables, but no data has been published for robust BOL/bump design rules for high temperature and high current conditions which is indigent in high performance packages. This project has been initiated to resolve EM challenges in the industry by identifying the BOL/ bump design with regards to the temperature/current conditions so a robust design rule/process window can be established for next generation packages.

Introduction

As flip chip continues its rapid advancement in the demanding markets, the complexities of devices are increasing exponentially. Challenges that the packaging industry faces include the need to deliver cleaner power to devices provide enough input/output (I/O) to accommodate the volume of data in high speed devices and still satisfy all other requirements without compromising reliability and/or cost. Bundling this much functionality into a single piece of advanced silicon requires a large interconnect gap between the silicon and the system printed circuit board (PCB) to be bridged.

Adoption of a copper (Cu) column fcCuBE® (flip chip package with Cu column bump, BOL interconnection and enhanced process) in place of flip chip solder bumps has number of potential benefits including bump pitch reduction, possible design rule relaxation by using wider line and space for signal routing in a given design, removal of tight solder registration, and the removal of solder on pad (SOP) on the substrate, all of which result in a low cost flip chip package solution [4-10]. The reduction in pitch capability is simply driven by the fact that bump to bump spacing can be controlled better with finer pitch Cu column as compared to a standard solder bump due to the bump geometry, spherical solder shape vs. cylindrical for Cu, and differences that exist in the bump geometry post reflow process. At the reflow step, solder collapses and an increase in bump diameter is observed, whereas Cu column will not go through any such transformation and will not experience any dimensional changes. Furthermore, the collapse height, which defines the die to substrate gap (stand-off height), can be better controlled by Cu column as the column height can be modulated to provide the required stand-off height without any increase in bump diameter, whereas any increase in stand-off height for solder bumps is associated with corresponding increase in bump diameter. Such an increase in bump diameter is not desirable as it would reduce the bump to bump spacing, resulting in potential bump bridging and electrical shorts. Additionally, the reduced bump to bump spacing would create issues for Capillary Underfill (CUF) flow and lead to underfill voids. Alternatively, it would create more voiding problem for the Molded Underfill (MUF) process due to a larger filler size used by the MUF material.

A motivation for using fine pitch Cu column bump is to improve the EM performance of the device due to the higher current carrying capability of Cu. However, Cu column on a very narrow pad becomes an issue due to the higher device power and current density which can be further aggravated due to the Joule heating effect ultimately leading to early EM failure.

Semiconductor companies are very concerned with the issue since it is a major source of failures today. An imminent solution is needed in order to overcome the industry-wide problem. In this study, EM test vehicles were designed with fine pitch Cu column and BOL design pad. The bump structures are exactly the same as actual product. The current flow direction in and out (with current pushing through three bumps and out one bump and vice versa) was designed in such a way that both the die side and substrate side failure can be captured in an actual EM test. The first degree of parameters such as BOL pad width, current condition, temperature conditions, BOL vs BOC (bond on capture pad, SMD pad type) pad type, etc. were considered in the DOE. EM failure data was collected and analyzed with statistical tools. Very comprehensive BOL/bump design rules and an optimum assembly process window were established to design a robust next generation Cu column package.

Package Design

Both the actual product and EM test vehicle followed the same design rule. In this particular device design, 40nm silicon was used with peripheral array bumps with 150um pitch. Package body size was a 17 x 17 mm package with 425 solder balls of 0.35mm diameter and 0.8mm pitch in four layers Plated through Hole (PTH) substrate. The die size was approximately 5.2 x 5.7 mm. Substrate core material was chosen as Low CTE material to control the package warpage/coplanarity in addition to extreme low-K (ELK) die protection. The gap between the bump to nearest trace is the

key for the fcCuBE design. Too narrow of a gap can cause assembly related issues such as solder bridging, shorting, etc.

Bumping process included PI re-passivation, Ti/Cu under bump metallization (UBM), and Cu column plating with a SnAg solder cap on top. As a result of this bumping structure, the peripheral bumps were located on the Al pads while the center mechanical bump array was located on the top passivation layer (no electrical contact). Figure1 shows the fcCuBE Cu bump and SnAg solder cap along with BOL trace detail for a given bump pitch design. Overall Cu column and solder cap height were optimized in order to create the optimum stand-off height required for successful CUF/MUF process in the assembly.

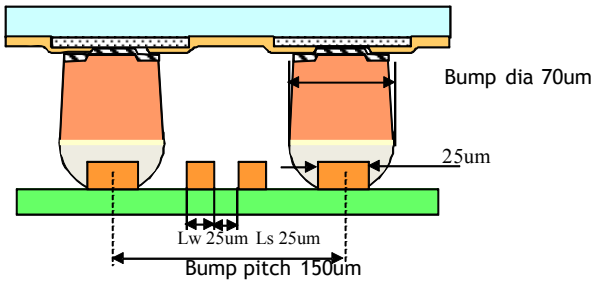

Figure 1: Bump pattern, and Cu pillar bump dimension detail w/ BOL pad

Assembly Process

The assembly process included several design iterations for bump height in order to optimize the CUF/MUF flow underneath the die. The original design with 42um column height with 35um solder cap encountered significant MUF voids. A modified design had 60um column height with 35um cap which enables a significant gap height increase. Higher column over solder cap ratio increased die level stress results in ELK crack (white bump) in actual product during the chip attach process. Significant ELK damage was experienced with taller column design even though it gives a better CUF/MUF process in the actual product. Figure 2 below shows white bump with taller column height with the actual product. Extensive simulation has been conducted to understand the safe limit of column/solder cap ratio. Finally, a design with 42um column and 35um solder cap with full open SR was introduced which maintained a smaller bump height to address the white bump issue. On the other hand, it increased the gap height significantly for void free MUF process.

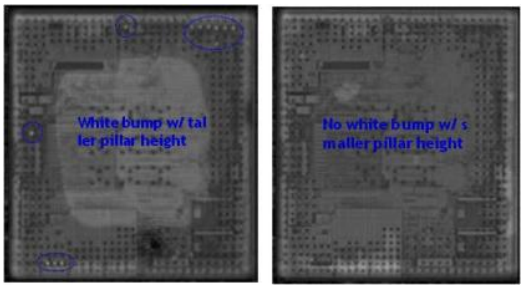

Figure 2: white bump w/ taller bump (left picture), and no white bump w/ smaller bump (right picture)

The detailed assembly process including flip chip attach, under-filling, overmold, ball attach, and singulation were fully optimized for assembly. The critical areas in the assembly process were identified as chip attach, molding, and ball mount processes. Additionally, an optimum amount of flux is needed in the chip attach process to make a good joint for very fine size/pitch Cu column. Die placement also plays a crucial role. If by any means the die are misaligned, solder bridging, non-wet, etc. might occurred in the chip attach process. Another important concern is white bump (bump delamination) for low K/ELK die. The white bump risk is much lower with the BOL pad versus BOC type pad. Having a smaller BOL pad helps to resolve the die level stress during the chip attach process by shifting the stress from die side to substrate side.

MUF process characterization focused on void free molding underneath the die. In this study void free MUF was one of the biggest challenges due to a finer diameter and a smaller gap height column. Moreover, the MUF filler size is much coarser than CUF, making the challenge even bigger. Today there are some finer filler MUF available in the market, but they have not yet achieved a preferred status for cost sensitive packages. Several iterations such as fine filler, taller bump height, and two step height solder resist, and an open solder resist under the die were used to fix the voiding issue. A comprehensive hammer test, MRT, and temperature cycles were conducted to authenticate void free design and process.

Electro-Migration Test

EM of bumps is a failure mechanism that leads to increased resistance, sometimes occurring with events such as formation of IMC, voids and cracks that can interrupt the bump joint and silicon, and/ or package metallization leading into the bump. The resistance increase can ultimately lead to a complete open in the device. The stress drivers for this type of failure mechanism are current density and elevated temperature. A motivation for using Cu column is to improve the EM performance of the device due to the higher current carrying capability of Cu. However, Cu column on a very narrow pad becomes an issue due to the higher device power and current density which can be further aggravated due to the Joule heating effect, ultimately leading to early EM failure

Bump level EM tests were performed both at in-house and a 3rd party vendor. EM test vehicle body size, die size, and bump structures were very similar to actual product. Current flow direction in and out (pushing through three bumps and out one bump and vice versa) was designed in such a way so both die side and substrate side failures can be captured in an actual EM test. Figure 3 shows the typical EM bump schematic for the three to one current flow condition. A dummy bump is attached between the functional bump to mimic the actual bump pattern in the product, moreover, dummy bumps help to normalize the “joule heating” effect during EM test.

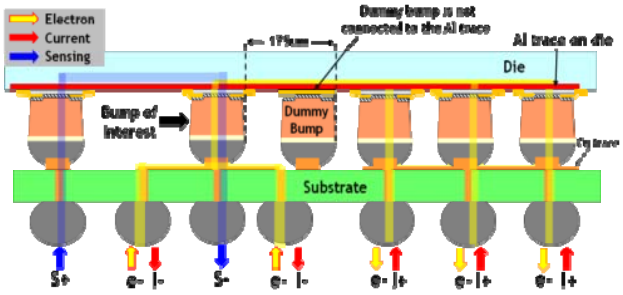

Figure 3: Typical EM bump schematic for 3 to 1 current flow condition

Actual electro-migration tests have been conducted both at in-house lab and a 3rd party vendor. Harsher condition legs were considered in the 3rd party vendor DOE than in house DOEs. The test matrix DOE is shown in Table 1 below. All samples have Cu column with 70um diameter and 52um gap height. Solder caps are 35um with 3 um thin Ni barriers between solder caps to Cu column. EM TV is very similar to actual product with 17X17mm body, 4 layer substrates with Cu OSP finish. The effect of the bump current flow in and out (3 in 1 out vs. 1 in 3 out) and BOL vs. BOC (bond on capture pad shown in Figure 4 below) pad were also considered in the DOE matrix. In order to create a Black's Model fit, a combination of at least five legs were used in the study. The devices under test (DUTs) were tested at constant current and temperature conditions. Actual device temperature will always be higher than oven temperature due to higher stress current and temperature (Joule heating effect). Therefore, Joule heating effect must be investigated and incorporated in the EM analysis. In this study, actual bump temperatures were derived using temperature coefficient of resistance (TCR) method. The average temperature increments due to Joule heating were added experimentally in each leg. Figure 5 shows a representative TCR result of the BOL structure at test with the condition of 150°C and 500 mA. The red box in Figure 5 shows the Joule heating on one DUT. Joule heating values of all the test conditions were less than 3°C

Test site	Leg#	Bump Composition	Bump net type	Temperature (C)	Stress current (mA)	Target testing hours	Comments
3rd party lab	1	Cu pillar w/ BOL pad	3 in 1 out	160	400	5000	DOE for Black's model fit
	2	Cu pillar w/ BOL pad	3 in 1 out	135	500		
	3	Cu pillar w/ BOL pad	3 in 1 out	150	500		
	4	Cu pillar w/ BOL pad	3 in 1 out	160	500		
	5	Cu pillar w/ BOL pad	3 in 1 out	160	650		
In house lab	6	Cu pillar w/ BOL pad	3 in 1 out	125	500	5000	DOE for Black's model fit
	7	Cu pillar w/ BOL pad	3 in 1 out	135	500		
	8	Cu pillar w/ BOL pad	3 in 1 out	150	300		
	9	Cu pillar w/ BOL pad	3 in 1 out	150	400		
	10	Cu pillar w/ BOL pad	3 in 1 out	150	500		
	11	Cu pillar w/ BOL pad	1 in 3 out	150	500		compare w/ leg#10
	12	Cu pillar w/ BOL pad	1 in 3 out	150	300		compare w/ leg#8
	13	Cu pillar w/ BOC pad	3 in 1 out	125	500		compare w/ leg#6

Table 1: EM Test DOE

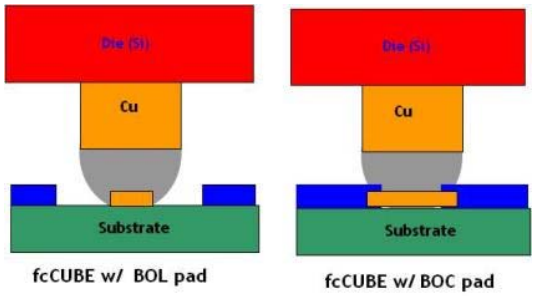

Figure 4: fcCuBE w/ BOL vs. BOC (SMD) Pad

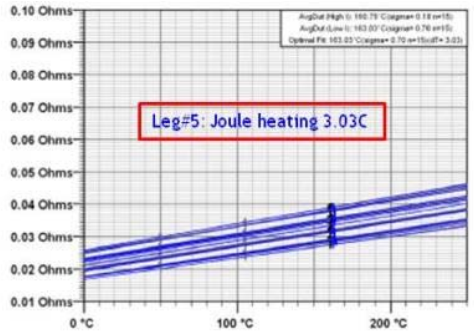

Figure 5: Typical TCR plot for BOL structure at 150°C, and 500 miliAmps stress current

The EM failure criterion was defined as the time at which a 15% increase in electrical resistance was observed. EM data was collected for over 7000 hours under accelerated conditions as indicated in Table 1. All samples have been tested over 7000 hours and no interconnection failures have been reported, however, we investigated interconnection morphologies induced by EM effects through cross-sectional analysis and analyzed the interfacial reaction characteristics between BOL and BOC structures for various stress conditions. The bump microstructures used in this test were observed with scanning electron microscopy (SEM) in the backscattered electron (BSE) mode, and the compositions of the resulting IMCs were measured by energy dispersive spectrometry (EDS).

EM Results

Over 7000 hours of EM test resistance shift data was plotted against stress time (hours). Figure 6 shows the resistance shift data for various temperature and current conditions. Based on resistance shift data, no failure was observed till 7000 hours which confirmed the robustness of the BOL bump structure in an fcCuBE package. The main objective was to collect adequate failure data to construct Black's equation which can be used as a tool for future package design optimization. However, no single failure was observed from any of the stress conditions.

Failure Analysis

Comprehensive failure analysis (FA) was conducted after 7000 hours of EM test to make sure there was no significant anomaly or crack in the interconnection area. A maximum 3% resistance shift was observed even with 650 miliAmps current at 160°C which confirms the robustness of fcCuBE bumps.

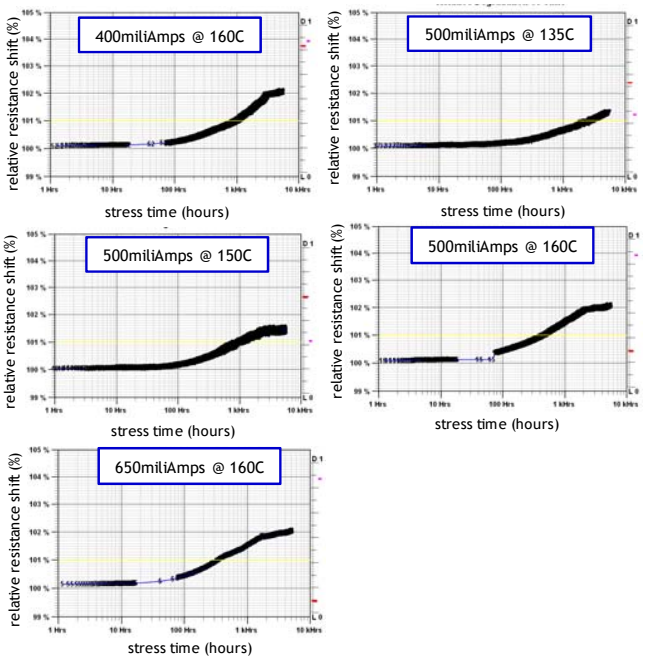

Figure 6: BOL resistance shift after 7000 hours for various test conditions

Two units from each leg were selected for destructive FA (failure analysis) and intermetallic morphology analysis. Figure 7 shows the location of the bump of interest and other bump structures in the EM package. No noticeable anomaly has been observed in the bumps after 7000 hours, as shown in Figure 7. Some minor voids due to solder diffusion were observed in the cross-section images. Detailed cross-section images for various legs were shown in Figure 8. Very thick IMC formed after 7000 hours of test. In the BOL structure very little solder was present in the bump compared to Cu Column. Almost the entire solder converted to IMC after 7000 hours of test. According to some literatures [3, 11] thicker IMC enhances EM performance. Some Kirkendal voids were also observed in the substrate pad to IMC interface (figure 8). Investigation found that Kirkendal void sizes have not been changed much over time. IMC thickness for each leg was also studied and analyzed per EM conditions. Over time SnAg solder was consumed by Cu. IMC thickness before and after EM were measured and plotted in Figure 9.

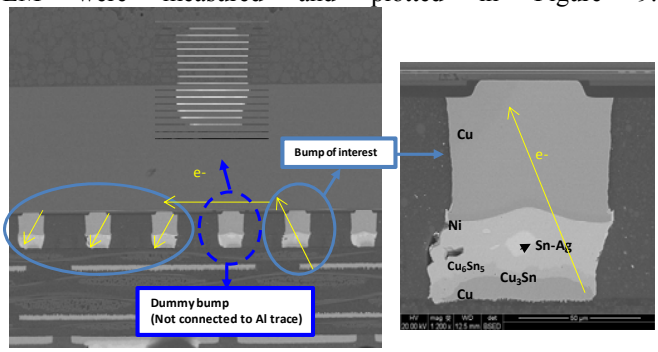

Figure 7: Detail X-section image of a unit (500 miliAmps @ 150^{0}C) after 7000 hours

The entire solder converted to IMC during EM testing. Very little IMC was observed in the Cu column interface due to presence of Ni barrier layer. No Cu diffusion took place in the column/solder interfaces due to Ni layer.

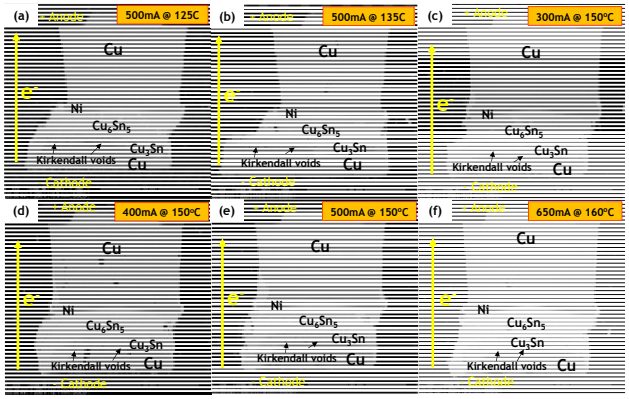

Figure 8: Cross-sectional images on each test condition after 7000 hrs: (a) 500 mA @ 125^{0}C, (b) 500 mA @ 135^{0}C, (c) 300 mA @ 150^{0}C, (d) 400 mA @ 150^{0}C, (e) 500 mA @ 150^{0}C, (f) 650 mA @ 160^{0}C

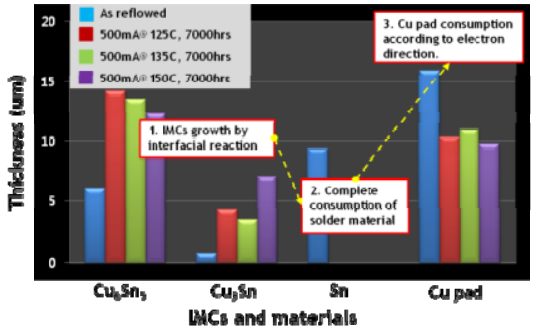

Figure 9: IMCs growth behaviors with three different temperatures (125^{0}C, 135^{0}C, and 150^{0}C) and 500 mA current conditions

The IMC growth mechanism in this study is illustrated in Figure 10. At reflow stage, Ni-Sn IMC was formed at the interface between the Ni layer and solder, and Cu-Sn IMCs were formed at the bonding interface between Cu pad and solder. During EM testing, the thickness of the Cu_6Sn_5 IMC increases until almost all Sn in the solder is consumed. Since the BOL structure has a limited amount of Sn and an infinite supply of Cu, Cu_3Sn IMC starts to grow thicker at the expense of Cu_6Sn_5 IMC. On the other hand, even though Ni_3Sn_4 IMC was formed at the interface between Ni/Sn after the reflow process, the Ni is a barrier layer to Cu and was not fully consumed during the EM test. This means that the Ni_3Sn_4 IMC barely grew; therefore Cu-Sn IMCs is the thicker IMC in interconnect.

BOL vs BOC Structure

EM occurs when the current density is sufficiently high enough to cause the drift of metal ions in the direction of the electron flow, and this is characterized by the ion flux density. Very high current can lead to a temperature gradient which is increasingly problematic and increasingly susceptibility to electro migration failures. Over design is one of the sources

for higher current density. Current density effect has been included and analyzed in the study. A naturally bigger pad is better for EM performance due to larger area. Current density is smaller for a bigger pad (BOC). There are a number of studies [4-10] with BOL pad in flip chip packages, but they do not compare EM performance between pad types.

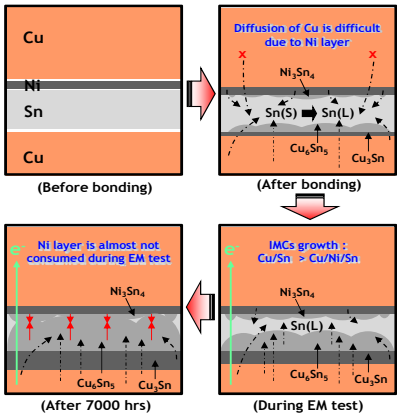

Figure 10: IMC formation mechanism and growth in the BOL structure combing Cu column and shallow solder bump

To compare EM characteristics between BOL and BOC Cu pad structures, an EM test on the BOC structure was also conducted under the same condition of 125^0C and 500 mA (leg#13, Table#1). No EM failure was observed in either BOL or BOC pad (till 7000 hours). Similar resistance shift behaviour was observed in BOC structure as well. However, an extensive bump cross-section has been conducted to analyse the interconnection degradation of BOL and BOC structure. Figure 11 illustrates the side by side bump interconnection degradation comparison between BOL and BOC structures. In the BOC structure, SOP was used on the substrate to attach the flip chip die. Hence, the BOC structure much more solder as compared to the BOL structure. In the BOC structure, Cu_6Sn_5 dominates everywhere due to huge amount of solder compared to Cu. The solder phase almost converted into Cu_6Sn_5 IMC. Furthermore, in the BOC structure, the substrate side Cu pad is entirely consumed by solder. Typically, current crowding during EM test significantly occurs at the cathode edge area and also the relatively uneven consumption morphology of the cathode Cu pad will cause incremental current crowding which was the case of BOC structure.

It was found that sufficient Sn in the BOC structure will induce high Cu consumption because Cu atoms from the pad can easily migrate into the widespread solder area. While BOL results showed that a significant number of Cu atoms remain due to limited solder area. In other words, the incidence of interfacial void and crack at BOC is more likely to occur at a higher rate than with the BOL structure (shown in Figure 11). Finally, both BOL and BOC structures used in this test did not show any electrical failure which means better EM reliability with an fcCuBE bump even with small BOL pad width.

Finally, current study with some legs as small as 25um BOL pad width showed no EM failure or interconnection abnormality till 7000 hours. Comprehensive failure analysis shows that even with 25um BOL width with as high as 600 miliAmps, stress current outperforms the BOC structure. One question remains unanswered; how small/narrow the BOL structure can be without sacrificing the EM reliability of the bump. A new study is being conducted with very narrow BOL pad (~15um) and high stress current (>500 miliAmps at 150^0C) which would answer the above question. Too high of current density can lead to early EM failure due to excessive Joule heating, metal migration, and brittle failure of bumps at the IMC (entire pad consumed by solder and become brittle IMC). A design limit of BOL pad size and stress current is being investigated to overcome the issues for very fine pitch Cu column bumps in the future very fine pitch packages.

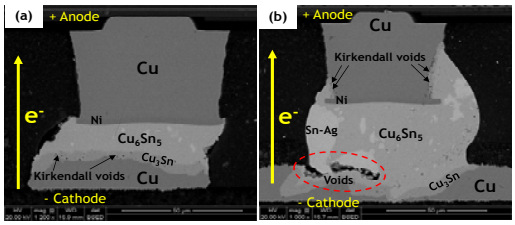

Figure11: Cross-sectional images of BOL (a) and BOC (b) under stress condition of 500 mA @ 125^0C after 7000 hrs

Conclusion

EM tests were performed on fine pitch Cu column BOL interconnections and BOC pad structure for various temperature and current conditions. Over 7000 hours of EM test were conducted and no failures were observed. Very insignificant resistance shifts were observed irrespective of current stress and temperatures. However, partial crack, solder diffusion, IMC thickness formation, etc were observed in the interconnection during EM tests. Thicker IMC forms on the substrate side (bond side) than Ni barrier side (Cu column side).

EM performance was compared between BOL and BOC pads for a given current stress and temperature. None of the pad structures failed. However, more interconnection degradation, IMC conversion, solder voiding, and partial cracks were observed in the BOC pad than BOL pad. It was found that the sufficient Sn in the BOC structure will induce high Cu consumption because Cu atoms from the pad can easily migrate into the widespread solder area. BOL results showed that a significant number of Cu atoms remain due to limited solder area. Typically, current crowding during EM tests significantly occurs at the cathode edge area and also the relatively uneven consumption morphology of the cathode Cu pad will cause incremental current crowding. Finally, BOL EM data proved that fcCuBE bump is much more robust for fine pitch high performance packages. Future programs with much higher current density (smaller BOL pad) for very fine pitch Cu column package is currently being conducted.

Acknowledgments

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