“Electrical-Thermal Characterization of Wires in Packages”

by

Kai Liu, HyunTai Kim, YongTaek Lee, Gwang Kim, Susan Park, and Billy Ahn
STATS ChipPAC

Robert Frye
RF Design Consulting, LLC

Electrical-Thermal Characterization of Wires in Packages

Kai Liu, Robert Frye*, HyunTai Kim, YongTaek Lee, Gwang Kim, Susan Park, and Billy Ahn

STATS ChipPAC
1711 W. Greentree Dr., Suite #117, Tempe, Arizona, 850284
kai.liu@statschippac.com, 480-222-1722
*RF Design Consulting, LLC

Abstract

The electrical-thermal co-simulation approaches, for wires-in-air and wires-in-package, are developed by the coupling between their electrical and thermal properties, using ADS (Agilent Design System) Symbolically-Defined Devices (SDD) models for multiple wire segments. Key parameters for these simulation models are then derived from experimental results. These experimentally validated (or assisted) simulation models can be used to predict electrical-thermal behavior of bond wires in situations of interest, and to develop design guidelines for reliable operation.

Test boards with wires-in-air were made, and fusing currents on wires of different materials (Au, Cu, Ag), lengths, and diameters were measured and compared with published data. Some QFN package testers having wires in different materials(Au, Cu, Ag), lengths, and different diameters, with mold material were also made to characterize the wires in real package environment. Simulation and experiment data, as well as some failure-analysis (FA) data through X-ray and SEM methods, are presented in the paper.

Introduction

Trends in package technology have led to the adoption of new materials and the use of smaller conductor geometries in package structures. Copper bond wires, for example, are used increasingly in place of gold wires. To accommodate increased numbers of die signal pads in smaller die sizes, chip designs use smaller pad-dimensions, requiring the use of smaller bond wire diameters in wire-bonded packages. These same trends have led to the adoption of smaller bump sizes in flip-chip designs and smaller line-width and space dimensions in package substrates.

On the other hand, trends in CMOS IC technology have also been toward smaller dimensions. To accomplish these changes in the physical dimensions of the transistors, it has been necessary (and desirable) to scale down the operating voltage of digital circuits. The general approach that has been adopted by the semiconductor industry is referred to as *constant power scaling*, in which the decreased operating voltages are accompanied by a proportional increase in overall operating current levels.

Together, these trends have led to appreciable increases in current density levels in the interconnecting conductors used in packages. Therefore, it is imperative that new design guide lines should be established to reflect these trends.

Many of the reliability concerns for package interconnection structures at high currents arise from the elevated temperatures that are developed as a result of resistive heating in the conductors. In contrast to electrical parameters, which can often be measured with great precision, thermal effects are much more difficult to precisely measure. This is especially true for very small structures like wire bonds or package traces. Because of their small thermal mass, temperature probes such as thermocouples or thermistors often perturb the result by conducting heat away from the Device Under Test (DUT). However, with reasonable simulation models, the DUT's thermal state can in many cases be inferred from its electrical behavior.

Thermal Circuit

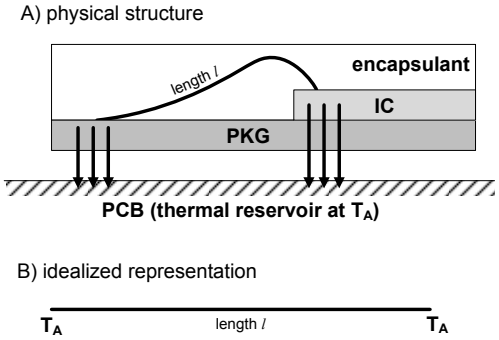

Figure 1. Typical bond wire package configuration and idealized representation**.**

Figure 1A shows a typical configuration for a bond wire in a package. The bond wire connects pads on the top surface of the IC to the underlying package. Heat is generated by the electrical resistance of the wire, the IC and the package, and flows into the underlying PCB, mainly through the electrical contacts, where it spreads out and is dissipated into the surrounding ambient. Typically, the package and PCB are very massive compared with the bond wire itself, and the resistance to thermal flow into the PCB is small. The dielectric encapsulation material (usually molding compound) surrounding the bond wire is a poor thermal conductor compared with the metal pathways, including the wire itself. So, especially near the ends of the wire, a key pathway for heat dissipation is via conduction along the length of the wire and through the package into the PCB. For analysis, the PCB itself is usually considered to be an infinite thermal reservoir at the ambient temperature, T_A. However, the overall thermal resistance of this conductive pathway grows with wire length. So, especially for longer wires, in the regions farther from the ends direct thermal conduction through the molding compound may be the dominant mechanism.

The heat flow equation for the case of an electrically-heated conductor in which the heat predominantly flows through the conductor itself is

$$\frac{\partial T}{\partial t} = \frac{k}{c_p \rho} \nabla^2 T + \frac{1}{c_p \rho} \vec{J} \cdot \vec{E} \tag{1}$$

The left-hand side of this equation is the time rate of change in the temperature, T. The first term on the right-hand side represents heat flow by conduction and the second represents electrical heat generation. In this equation, c_p is the heat capacity at constant pressure, ρ is the density and k is the thermal conductivity. The electrical power dissipated in the material is given by the scalar product of the current density, J, and the electric field, E. More generally, a third term on the right-hand side would be included to account for radiated power, but this is assumed to be negligible in this case.

In an electrically conducting material the current density and electric field are related by Ohm's law

$$\vec{J} = \sigma \vec{E} \tag{2}$$

where σ is the electrical conductivity. In this case, Equation (1) becomes

$$\frac{\partial T}{\partial t} = \frac{k}{c_p \rho} \nabla^2 T + \frac{1}{c_p \rho} \frac{J^2}{\sigma}. \tag{3}$$

Figure 1B shows a highly idealized representation of the bond wire that is used for analysis. It is assumed that the thermal resistances of the pathways from the wire ends into the PCB are low compared with the resistance of the wire itself, and can be neglected. In this case, the ends of the wire

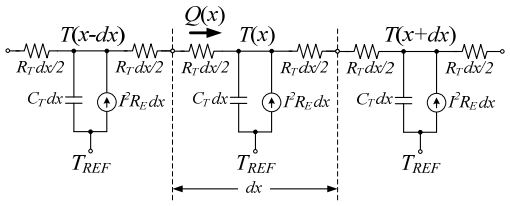

Figure 3. Distributed thermal circuit model.

can be assumed to be at the ambient temperature T_A. Furthermore, additional dissipation by conduction into the surrounding encapsulation material is assumed to be negligible. In this case, the only heat flow is along the length of the wire, and the heat flow equation is one-dimensional:

$$\frac{\partial T}{\partial t} = \frac{k}{c_p \rho} \frac{\partial^2 T}{\partial x^2} + \frac{1}{c_p \rho} \frac{J^2}{\sigma} \tag{4}$$

For uniform current density through a wire of cross-section area A, Equation (4) becomes

$$\frac{\partial T}{\partial t} = \frac{k}{c_p \rho} \frac{\partial^2 T}{\partial x^2} + \frac{1}{c_p \rho} \frac{I(t)^2}{A^2 \sigma} \tag{5}$$

where $I(t)$ is the total current flowing through the wire. It is assumed that the current is only a function of time, and is uniform along the wire's length.

Solutions of the heat-flow equation describe wave-type behavior for the temperature distribution. It has long been recognized that flow of heat in response to gradients in the temperature is directly analogous to the flow of charges (electrical current) in response to gradients in the potential (electrical voltage). Furthermore, heat flow can be modeled using circuit element concepts [1]. For this one-dimensional heat flow problem, we can define several circuit-element analogs.

We define the thermal capacitance per unit length to be

$$C_T \equiv c_p \rho A \tag{6}$$

The thermal resistance per unit length is defined as

$$R_T = \frac{1}{kA} \tag{7}$$

and the electrical resistance per unit length as

$$R_E \equiv \frac{1}{\sigma A} \tag{8}$$

With these definitions, Equation (5) becomes

$$C_T \frac{\partial T}{\partial t} - \frac{1}{R_T} \frac{\partial^2 T}{\partial x^2} = I^2 R_E \tag{9}$$

The left side of this equation is identical in form to the electrical equations describing voltage propagation in a distributed RC delay line. In this equation, the temperature T is analogous to the voltage in an electrical circuit. At any point along the distributed line, the first term represents a "current" (actually heat flow) flowing out of that point through a shunt capacitance. The second term represents the net heat flow out of that point through the series resistance.

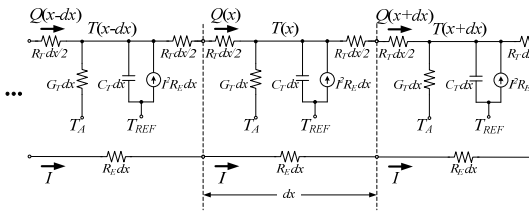

Figure 2. Coupled thermal-electrical circuit model**.**

The right-hand side of the equation is a heat-flow current that

is injected into the region (i.e. a source) representing the electrical joule heating.

Figure 2 shows a distributed circuit representation of the heat flow equation. In this circuit, the node voltages represent temperatures and the branch currents represent heat flows. The length of the wire bond is subdivided into incremental sections of length dx, and the lumped circuit elements are calculated from the per-unit-length parameters described in Equations (7)-(9). The reference temperature T_{REF} in this circuit is analogous to the ground potential in an electrical circuit.

The one-dimensional heat flow equation (Equation (9)) assumes that the only appreciable mechanism of heat flow is along the wire. In practical situations, however, some of the heat is removed into the material surrounding the wire, typically molding compound or, in the case of some of the experimental results, air. This mechanism becomes more important for longer wires. The resistance to heat flow into the surrounding material is the same at all points along the length of the wire, but the resistance to heat flow out the ends of the wire grows with distance from the ends. The modified version of Equation (9) that accounts for this is

$$G_T\left(T-T_A\right)+C_T\frac{\partial T}{\partial t}-\frac{1}{R_T}\frac{\partial^2 T}{\partial x^2}=I^2R_E \qquad (10)$$

where G_T is a thermal conductance per unit length. For a cylindrical wire of diameter d, the thermal conductance for heat transfer into an infinite surrounding medium is typically represented by

$$G_T=\pi dh \qquad (11)$$

where h is the heat-transfer coefficient. In this model it is assumed that the heat transfer is proportional to the outer surface area of the wire and the local temperature difference between the wire and the ambient. Unlike the other parameters, the heat-transfer coefficient is not an intrinsic property of the wire material. Instead, it depends mainly on the nature of the surrounding medium.

Figure 3 shows the coupled electrical-thermal simulation model. In this circuit model, the lower part represents the electrical pathway through the wire, and the upper part represents the thermal pathway. The main coupling between the two is via the dependent sources that drive "current" (i.e. heat) into the thermal part of the circuit that is proportional to the electrical power generated in each section. Further coupling occurs that is not shown, since the electrical resistance R_E is dependent on the temperature. This is one of several nonlinear effects that must be included in the model.

Nonlinear Effects

Equation (9) is a linear partial-differential equation, and can be solved analytically for the simple boundary conditions described in Figure 1. However, a careful examination of the material properties of the metals used in bond wires shows that the key thermal and electrical parameters are, themselves, temperature-dependent. This makes the equations nonlinear.

The electrical conductivity, for example, shows a large variation with temperature. Over the range from room temperature to the melting temperature, the electrical resistivity of metals is reasonably well described by a first-order behavior. This dependence is given by

$$\sigma=\frac{\sigma_0}{1+\alpha\left(T-T_{REF}\right)} \qquad (12)$$

where σ_0 is the conductivity at temperature T_{REF} and α is the temperature coefficient of resistance. Typically, these parameters are defined at a reference temperature of 20C. For the calculation of fusing currents, the nonlinear variation in electrical conductivity is a significant effect. At its melting temperature, the conductivity of the metal is typically only 25-30% of its value at room temperature.

The thermal conductivity also shows variation with temperature, and over the range from room temperature to the melting point it can also be represented by a first order dependence

$$k=k_0\left[1+\beta\left(T-T_{REF}\right)\right] \qquad (13)$$

where k_0 is the thermal conductivity measured at temperature T_{REF} and β is the first-order temperature coefficient of the thermal conductivity. Like the electrical conductivity, the thermal conductivity of bond wire metals decreases with increasing temperature, so β is negative. However, the magnitude of the effect is less. Typically the thermal conductivity at the melting temperature is 5-10% less than at room temperature.

Finally, the heat capacity of the metal shows a similar dependence

$$c_p=c_{p0}\left[1+\gamma\left(T-T_{REF}\right)\right] \qquad (14)$$

Heat capacity also increases slightly with increasing temperature.

It is also the case that the density is temperature dependent. This is related to the coefficient of thermal expansion. But this effect is relatively minor compared with the above effects and can be ignored in this analysis. Table 1

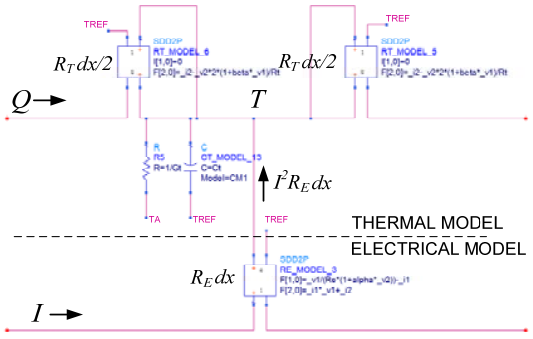

Figure 4. Agilent ADS implementation.

lists values for the nonlinear effects described above in pure metals, derived from a variety of sources [2]-[4].

Table 1. Material parameters for pure metals at T_{REF}=20C.

Parameter	Units	Ag	Au	Cu
σ_0	Sm^{-1}	$6.30\cdot10^{7}$	$4.10\cdot10^{7}$	$5.95\cdot10^{7}$
α	K^{-1}	$4.31\cdot10^{-3}$	$3.73\cdot10^{-3}$	$3.93\cdot10^{-3}$
k_0	$Wm^{-1}K^{-1}$	427	315	398
β	K^{-1}	$-1.82\cdot10^{-4}$	$-1.87\cdot10^{-4}$	$-1.56\cdot10^{-4}$
c_0	$Jg^{-1}K^{-1}$	0.230	0.126	0.386
γ	K^{-1}	$1.93\cdot10^{-4}$	$2.39\cdot10^{-4}$	$2.49\cdot10^{-4}$
ρ	gm^{-3}	$1.05\cdot10^{7}$	$1.89\cdot10^{7}$	$8.94\cdot10^{6}$

When these more accurate temperature-dependent material parameters are used, Equation (5) is nonlinear and cannot be solved analytically. To circumvent this difficulty, in an analysis of fusing time and current Loh [5] effectively used a more approximate form in which these parameters were replaced by their average value over the temperature range of interest, such as,

$$\frac{I^2}{\bar{\sigma}A} = -A\bar{k}\frac{d^2T}{dx^2} + A\rho\bar{c}_p\frac{dT}{dt} \tag{15}$$

In addition, Loh's analysis focused on the calculation of the fusing time. In the more general case, we are interested in a detailed analysis of the spatial distribution of the temperature along the wire at lower temperatures. This makes it possible to determine the changes in the observed wire resistance, which can be used to relate experimental observations with the peak temperatures in the wire.

An advantage of the thermal circuit model is that it can be conveniently implemented in an electrical circuit simulator to find the transient behavior of the temperature, taking into account the nonlinear effects. An additional advantage, as will be seen, is that the thermal circuit model is easily extended to include the effects of non-ideal boundary conditions, which are difficult to achieve in practical measurements.

Simulation Methodology

The coupled flow shown in the model in Figure 3 can be implemented in a transient circuit simulator such as Agilent ADS. The basic circuit implementation for the incremental length of line described above is shown in Figure 4. In this circuit, the two-port block elements are Symbolically-Defined Devices (SDD) from the "Eqn Based-Nonlinear" palette of ADS. The upper part of the circuit models the heat flow path along the wire, and the bottom half models the electrical charge flow path.

In the ADS implementation, the incremental, temperature-dependent electrical resistance, R_E, and thermal resistance, R_T are represented by the SDD blocks. Furthermore, the block representing R_E generates an output "current" at port-2, representing the heat flow into the thermal part of the circuit.

In the SDD block representing R_E, the net voltage on port-2 is

$$\_v2 = T - T_{REF} \tag{16}$$

The "current" (i.e. heat flow) from port 2 of the R_E block is equal to the power dissipated in the electrical part (port-1) of the circuit:

$$\_i2 = -\_v1 * \_i1 \tag{17}$$

The minus sign in the right-hand side of Equation (17) takes into account the fact that positive power in port-1 should cause current to flow *out* from the positive terminal of port-2. In the ADS convention, this corresponds to negative current. Equation (17) is implemented in the ADS SDD component using the implicit relationship

$$0 = \_i2 + \_v1 * \_i1 = F(2,0) \tag{18}$$

Port-1 of this device represents the temperature-dependent electrical resistance of the line segment, which is given by

$$R_E = \frac{dx}{\sigma_0 A}\left[1 + \alpha\left(T - T_{REF}\right)\right] \tag{19}$$

In the SDD device, using Equation (10), the equation defining the electrical characteristics of port-1 is

$$\_i1 = \_v1 / R = \_v1 / \left[Re * (1 + alpha * \_v2)\right] \tag{20}$$

where

$$Re = \frac{dx}{\sigma_0 A} \tag{21}$$

The implicit relationship for port-1 is

$$0 = \_v1 / \left[\mathrm{Re} * (1 + alpha * \_v2)\right] - \_i1 = F(1,0) \tag{22}$$

The two SDD blocks in the upper part of the circuit represent the two nonlinear thermal resistances in Figure 3. Port-1 of these devices only senses temperature. The voltage across this port is given by

$$\_v1 = T - T_{REF} \tag{23}$$

No current flows in this port, so the explicit equation describing its I-V characteristics is

$$I(1,0) = 0 \tag{24}$$

Port-2 represents the thermal resistance. Its voltage-current relationship is given by

$$\_i2 = \_v2 / (R_T / 2) = 2 * \_v2 * (1 + beta * \_v1) / Rt \tag{25}$$

where

$$Rt = \frac{dx}{k_0 A} \tag{26}$$

Table 2: Measured parameters of the wires at low current.

Metal	d_{NOM} (mil)	σ_{NOM} (S/m)	R_E (Ω/m)	d_{EFF} (mil)	σ_{EFF} (S/m)	R_{PKG} (mΩ)
Au-99	1.0	3.42e7	82.7	0.83	2.46e7	6.07
	0.6		206.2	0.53	2.75e7	14.14
Pd-coated Cu	1.0	5.57e7	38.3	0.96	5.32e7	4.32
	0.6		112.5	0.56	5.03e7	8.37
Ag-88	1.0	2.00e7	104.8	0.97	1.94e7	7.94
	0.8		167.5	0.77	1.90e7	9.09
Ag-96	1.0	3.57e7	65.8	0.92	3.10e7	6.89
	0.8		106.1	0.72	3.00e7	7.19

The final nonlinear element in the co-simulation model is the thermal capacitance. In ADS this is most conveniently implemented as a simple nonlinear capacitance. The "voltage" (i.e. temperature) across the capacitor is T-T_{REF}. Consequently, the linear temperature coefficient of the heat capacity, γ, is equivalent to the linear voltage coefficient of capacitance in the electrical analog. This is implemented by the capacitor model element CM1 in the simulation.

The thermal conductance per unit length, G_T, is a linear element in the model. It is implemented by a simple resistance connecting the thermal node, at temperature T, to the ambient at temperature T_A. Similar to the reference temperature, the ambient temperature is set by a dc source in the simulation.

The model element shown in Figure 4 represents a short segment of the bond wire. The overall model is built up from a cascade of these elements (typically ten segments). These parts of the simulation represent the bond wire. Additional model elements are needed to account for the thermal and electrical boundary conditions of the physical structure. For example, the experimental sample may also introduce additional contact resistances in the electrical path of the model and additional thermal resistance in the thermal path. A key advantage of the electrical-thermal co-simulation methodology described above is that these boundary conditions can easily be added or modified to suit the circumstances of each particular experiment. The details of these boundary conditions are discussed in the following sections describing the experiments.

QFN-Mounted Samples

Figure 5 shows the bonding diagram for the QFN packages. Each package contained 8 wires bonded from one of the QFN pins to the central die paddle of the packages. As shown in the diagram, the wires had a nominal length of 1, 2, 3 and 4mm. These packages were assembled using automated wire bond equipment. The loop height and end-points of the wires were adjusted so that the actual wire length closely matched the nominal length. The one exception to this was the 4mm wire which, because of equipment limitations, had an actual length of 3.9mm.

Eight different wire types were measured in these tests: Au-99 wire of 1-mil and 0.6-mil diameters, Pd-coated Cu wire of 1mil and 0.6mil diameters, Ag-88 wire of 1-mil and 0.8-mil diameters and Ag-96 wire of 1-mil and 0.8mil diameters. The material and model parameters used in the simulation comparisons are listed in Table 2.

The package pins of the QFN-mounted samples are large, allowing the use of 4-point probe contact. The QFN package itself was mounted upside-down on the chuck of a probe station. A metal block that served as a heat sink was clamped onto the package such that it covered most of the exposed center pad of the package. Two high-current probes were used to supply the test current to the samples, and the voltage was measured through a second pair of finer probes connected to the package terminals.

The four-point probe eliminates the probe electrical resistance from the measurement, so there was no need to characterize the fixture. This has the further advantage of eliminating the variable contact resistance. The metal block that forms the heat sink has a very large thermal mass, so the paddle of the QFN package can be assumed to be held at ambient temperature.

Because the wire lengths were well-controlled in these samples, it was possible to very accurately determine the resistance per unit of the wires. This was done by finding a linear least-squared error fit to the measure resistance at low

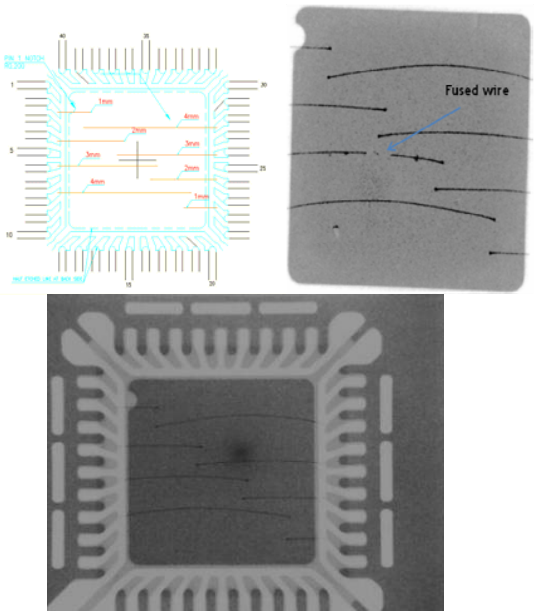

Figure 5. Bonding diagram for the QFN-mounted samples (top left), and X-ray picture after fusing test on 3mm long wire (top right). Tester QFN package with wires for measurement (bottom).

Table 3. Fitted thermal conductance values.

Metal	Diameter (mil)	G_T, QFN ($WK^{-1}m^{-1}$)	G_T, air ($WK^{-1}m^{-1}$)
Au-99	1	1.5	0.090
	0.6	1.5	0.054
Pd-coated Cu	1	1.2	0.090
	0.6	1.2	0.054
Ag-88	1	1.5	0.090
	0.8	1.5	0.072
Ag-96	1	1.7	0.090
	0.8	1.7	0.072

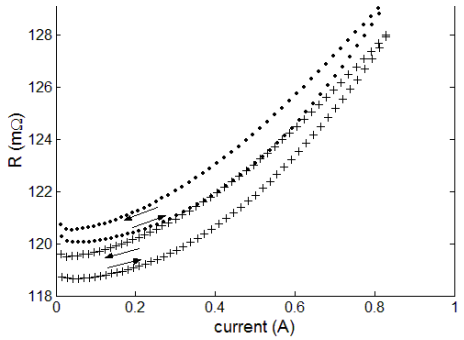

Figure 6. Example resistance versus current result from a QFN-mounted sample (3mm-long 1-mil Pd-coated Cu wire).

current as a function of the wire length. The slope of this fit gives the resistance per unit length and the intercept gives the parasitic resistance of the package leads. These measured values are listed in Table 2.

Table 2 shows the nominal metal conductivity, σ_{NOM}, and nominal wire diameter, d_{NOM}. In all cases we observed that the measured wire resistance per unit length, R_E, is slightly higher than expected based on the manufacturer's specifications for the metal resistivity. We speculate that this is likely a result of the wire drawing process, which alters to some extent the grain structure of the metal compared with its original bulk form. (The resistivity is characterized by measurement of the bulk material, not the wire.) As mentioned above, some of this variation may also be a result of variation in the actual wire diameter, which is specified to a tolerance of ±1μm. The observed higher resistance may result from either reduced effective conductivity (σ_{EFF}) or reduced effective wire diameter (d_{EFF}) or a combination of these effects. But since in all cases the resistance was higher than expected, we believe that the more likely explanation is that the conductivity is reduced. This effect is especially pronounced in the gold wires. However, the simulation result is equivalent using either a reduced effective diameter or electrical conductivity.

A simple ramp-up, ramp-down sequence of applied current was used in these measurements. The maximum current used in the tests was based on the previous results from PCB-mounted samples, and was intended to result in a maximum wire of about 200C. Figure 6 shows a typical result. In all cases the resistance versus current showed a small hysteresis, most likely arising from some temperature increase in the heat-sink block. Since the overall resistance in these samples is dominated by the wire itself, from the relative difference between the ramp-up and ramp-down curves we can estimate that this hysteresis corresponds to about a 2-degree difference in the wire temperature, which is negligible. In addition, in all of the measurements the resistance versus current curves have negative slope at low current. This is almost certainly an experimental artifact, perhaps resulting from a small temperature dependence in the external current sensing resistance. In the worst case, it results in a relative drop of 0.5% in the low current resistance.

One reason that these effects are so apparent in the data is that the overall temperature rise in the wires is much smaller than expected. In the example shown in Figure 10, the relative change in resistance is about 8%. This indicates that the average wire temperature increases by about 20ºC above ambient at a current of 800mA.

The coupled thermal-electrical model shown in Figure 3 can be applied to QFN-mounted samples. As discussed above (Equation (10)), in the steady state, the time rate of change is zero. In this condition the heat balance, Equation (10) becomes

$$I_{MAX} = \sqrt{\frac{G_T}{R_E}\frac{(T_{MAX} - T_A)}{\left[1 + \alpha(T_{MAX} - T_{REF})\right]}} \qquad (27)$$

Max current depends only on the electrical resistance per unit length and the thermal conductance per unit length from the wire to the ambient. In the case of a wire in air (as in the standard fusing current test) the thermal conductance per unit length is determined by convection. In that case, heat is transferred to air molecules where the physical processes of conduction and diffusion transport the heat away from the wire. In the case of the QFN packages, heat is transported from the wire mainly into the nearby package paddle, which is near the ambient temperature. The molding compound, which is much more thermally conductive than air, acts as the medium for the heat conduction.

Using the electrical resistance per unit length derived from the low-current limits of the measurements (Table 2) and the same value of probe thermal resistance as in the PCB-mounted measurements (120ºK/W) previously done, the only remaining parameter to be fitted is the thermal conductance per unit length, G_T. For convective cooling in air, G_T is typically assumed to be proportional to the wire's diameter (Equation (11)) but in the case of the molded package, we would expect that the conductance depends on proximity to the cool paddle, so its dependence on diameter is not so obvious. The approach used in interpreting these measurements is to determine for each wire type the value of G_T that best fits simulation to measurement. In addition, it can be seen in the package diagram in Figure 5 that for part of its length the wire does not lie immediately above the package paddle. In the model this region is assumed to have negligible conductance.

The experimental results, along with simulations using fitted values of G_T from this simulation model are shown in

Figure 7. The fitted values of G_T are shown in Table 3. Because the overall temperature rise in these samples was low and the resistance change is small. Consequently, these data can be reasonably well modeled by a range of values of G_T. In fusing experiments, the data spans a much wider range of temperature and resistance change, and in those measurements the value of G_T is much less ambiguous. For this reason, the values of G_T used in the simulations are derived from the fusing experiments, and the method used for this derivation will be described in a subsequent section. These values are listed in Table 3. For comparison, the values obtained in the PCB samples for another project are also listed.

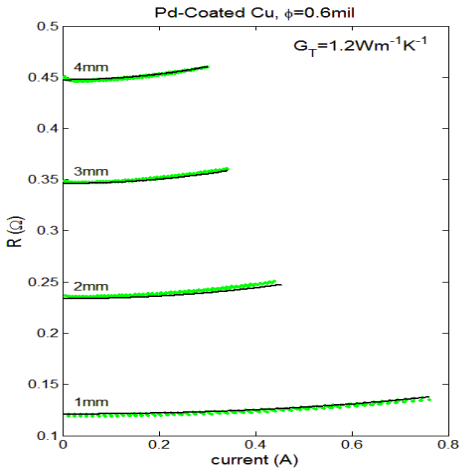

Figure 7. Resistance versus current relationship for QFN-mounted Pd-coated Cu wires. Green lines from measurement, and black lines from simulation.

The differences in the magnitude of the thermal conductance values are apparent in this table. Thermal conductance in molded packages is more than an order of magnitude greater than in air. There are other interesting differences as well. Whereas thermal conductance via convection in air is proportional to the wire diameter, it appears on the basis of these measurements that in the molded packages the thermal conductance is independent or very weakly dependent, on diameter. In air, the thermal conductance does not depend on the wire material, but it appears that in the case of the molded packages it does.

A key consideration in the fitted values of G_T is the distance between the wire and the package paddle. We would expect that as this distance decreases the thermal conductance should increase. The model assumes a single value for the entire length of the wire when, in fact, the distance tapers to zero at the point of the wire attachment to the paddle. Nonetheless, it appears that the observed behavior is well-explained by these conductance values, which may be considered to be an effective, average conductance over the wire length.

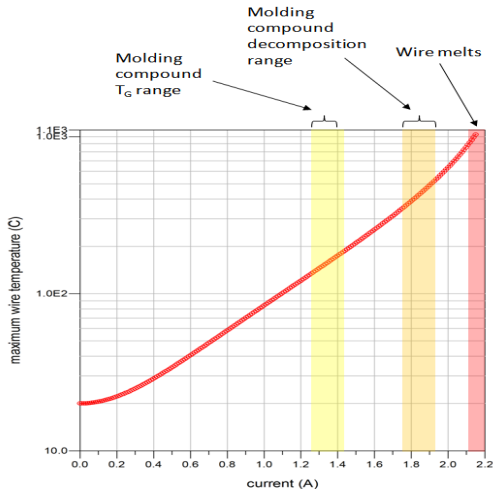

Figure 8. Simulated maximum wire temperature versus current for a 3mm long, 1-mil diameter Au-99 wire in a QFN package.

Current Capacity Guidelines for Wires in QFN Packages

Using the model values derived from these samples, we can run simulations to find the maximum internal wire temperature as a function of applied current, and extrapolate these results to higher currents. An example result is shown in Figure 8. It can be seen in this figure that the maximum wire temperature increase is approximately exponential with applied current. Figure 9 shows the wire temperature as a function of distance along the wire, from the thermal-electrical simulation.

The temperature profiles in this plot show that the point of maximum wire temperature is located near the mid-point of the wire length, but slightly closer to the pin connection, which is slightly hotter than the package paddle. The three current levels shown in this plot correspond, approximately, to the lower limit of the three temperature ranges identified in Figure 9. Especially at the lower current levels, the temperature profile near the wire midpoint is very flat. Because there is little temperature gradient along the wire, this indicates that there is little heat flow along the wire's axis. The main mechanism of cooling in this case is thermal conduction through the molding compound into the package paddle, and the temperature in this section is approximately described by the long-wire limit.

From failure analysis lately done, even before the wire was driven at fusing current, the molding material was decomposed (Figure. 10). In other words, the wire will not fail before the molding material does. Therefore we use temperature below Tg of the molding material as the maximum temperature to safely provide a guideline.

The results listed in Tables 2 and 3, in particular the values of R_E and G_T, can be used to predict the maximum temperature rise in long wires. These may be considered to be worst-case estimates, since shorter wires will generally be somewhat cooler than longer ones for a given current. The maximum current in long bond wires as a function of the maximum allowable wire temperature is given by Equation (27).

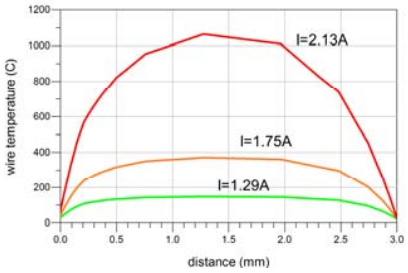

Figure 9. Example simulated wire temperature as a function of distance along the wire for a 3mm-long 1-mil diameter Au-99 wire bond in a QFN package. In this plot the wire connection to the package pin is on the left**.**

The experimental results in this study were obtained at ambient temperature of about 20C, which is also the reference temperature for the resistance. For the specification of maximum current guidelines, it is necessary to consider worst-case operating conditions of higher ambient temperature. For industrial applications it is typically 85C. Table 4 lists values of maximum operating current for various values of maximum wire temperature in the long wire limit for typical industrial applications.

Conclusions

The thermal conductance per unit length is much higher than in air. This is to be expected, since the molding compound is generally much more thermally conductive. The unexpected result, however, is that the conductance is independent of the wire diameter, at least within the limits of the accuracy to which we are able to resolve it. The other unexpected result is that the thermal conductance appears to depend on the wire material(Au, Cu, Ag). This result suggests that interfacial characteristics between the bond-wire metal and the molding compound may play a role in this heat transfer. It can be seen in Table 3 that values of G_T for palladium-coated copper wire are significantly different than those for gold wire of the same diameter.

Table 4. Maximum current capacity guidelines for ambient temperature of 85C (industrial**).**

Metal	Diameter (mil)	Maximum Current (A)		
		T_{MAX}=100 C	T_{MAX}=125 C	T_{MAX}=150 C
Au-99	1	0.47	0.74	0.92
	0.6	0.30	0.47	0.58
Pd-coated Cu	1	0.60	0.95	1.17
	0.6	0.35	0.55	0.68
Ag-88	1	0.44	0.71	0.89
	0.8	0.35	0.56	0.70
Ag-96	1	0.57	0.91	1.13
	0.8	0.45	0.71	0.89

The experiment-assisted simulation method simulates very fast (in few seconds) and predicts the wires' thermal and electrical behaviors reasonably well. When wires are in

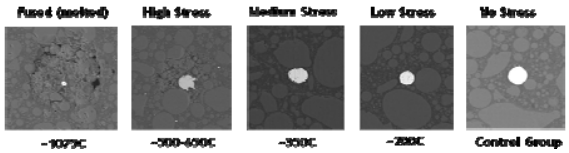

Figure 10. Damage signatures of wires in a QFN package driven at different currents.

molding material of a package, they will not fail before the molding material does, as Tg temperature and decomposition temperature of molding material are much lower than melting temperature of a metal wire. The maximum current capacity guidelines listed in Tables 6 are the main significant result of this investigation, and designing within these guidelines is necessary for long-term reliability.

Acknowledgments

The current-driven tests for this project was done by Robert Melville at Emecon, LLC. The authors are grateful for the help of Linda Chua at STATS ChipPAC, Singapore in the preparation of experimental samples.

References

1. K. W. Awkward, "Model for determining thermal profiles of bond wires using 'PSICE' analysis", *Proc. IEEE SEMI-THERM* VII, 86-90, Feb 1991, pp.12-14.
2. E. Loh, "Physical Analysis of Data on Fused-Open Bond Wires," *IEEE Trans. Components, Hybrids and Manufacturing Technology*, **CHMT-6**, No. 2, JUne 1983, pp. 209-217.
3. R. W. Powell, C. Y. Ho and P. E. Liley, "*The Thermal Conductivity of Selected Materials*," National Standard Reference Series, NSRDS-NBS 8, 1966.
4. S. I. Abu-Eishah, Y. Haddad, A. Solieman and A. Bajbouj, "A New Correlation for the Specific Heat of Metals, Metal Oxides and Metal Fluorides as a Function of Temperature," *Latin American Applied Research*, **34**, 2004, pp. 257-265.
5. R. C. Dorf, ed. *The Electrical Engineering Handbook*, CRC Press, ISBN 0-8493-0185-8, 1993.
6. A. Teverovsky, "Effect of environments on degradation of molding compound and wire bonds in PEMs", *Proc. 56th Electronic Components and Technology Conference*, 2006.