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Warpage Mitigation Processes in the Assembly of Large Body Size Mixed Pitch BGA Coreless Packages for Use in High Speed Network Applications.

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Abstract

Next generation high speed network ASIC packages require perpetually larger and thinner packages to meet functionality and electrical performance requirements. Opportunities for highly integrated MCM's and 2.5D/3D Si interposer packages are emerging to meet long-term performance needs, but for near-term, single chip ASIC applications, thinner packages utilizing thin substrates are an absolute requirement for the high end network market. Achieving both increased margins in the power delivery network and increased functionality in next generation 25/28GHz ASIC applications requires highly efficient (thin, minimal discontinuities, opportunities for enhanced decoupling), low loss package designs with package sizes up to 60x60mm. Coreless substrate based packages offer an excellent opportunity for low loss/low inductance package designs, but have consistently failed to be available at the necessary body sizes due to assembly and warpage concerns. The work presented in this paper describes key factors for mitigating warpage and identifies optimum processes, and materials for manufacturing large body size coreless substrate packages, especially for the high end network market.

A test vehicle was developed using a 22x18mm², 40nm Daisy Chain die placed onto a 45x45mm², 8+1 coreless substrate with mixed pitch BGA footprint and BGA-side capacitors. Processes were developed to optimize assembly yield and package reliability. Key assembly materials were selected for optimum yield and high thermo-mechanical reliability. Substrate material stack-up and design were varied for further optimization and validation of thermal mechanical reliability models. As a result, critical factors impacting warpage were identified and modeling tools were refined to predict substrate.

This paper describes the assembly processes, substrate BOM selection and design strategies adopted for mitigating warpage for coreless package sizes up to 45x45mm. Additionally, L1 thermal mechanical reliability results and key factors for establishing valid models will be discussed.

Key Words

Coreless, mpBGA, warpage, ASIC, assembly process.

Introduction

As the "network as a platform" continues to evolve supporting the convergence of various multi-media sources and collaboration tools, the demand that is placed on the architecture, hardware, and software that makes this level of connectivity possible, pushes the limits of current assembly and design capability. High-end networking and computing applications drive silicon technologies for higher data rates and increased bandwidth. The greater functionality and processing speeds required of today's networking ASIC's has driven flip chip packaging technology into previously untested realms of ultra-low k Si, very large package size, high substrate layer count, Pb-free solder, and thin package/core thickness. Furthermore, many of the next generation devices are high powered (>100W) components requiring unique heat dissipation strategies and are many times implemented in remote, uncontrolled environments. These factors are challenging existing packaging materials and assembly capability, printed circuit (PC) assembly capability and overall package and system level reliability. At the current rate at which Si node is advancing, packaging technology is refined every 2-3 years; this puts a burden on the component and PC assembly industries to keep up.

Motivation

The rate and volume of data transfer through an interface (i.e. bandwidth) is a key factor in determining network performance. High bandwidth devices require consistent and steady supply of power even through sustained switching events in order function properly. As the devices become more functional through the evolution of the various silicon nodes, the power integrity of the device becomes strained as the supply voltages and related noise margin drop. One of the goals of an optimally designed power delivery network (PDN) is to maintain as low impedance as possible. Forming direct, electrically short and multiple redundant contacts is one way to achieve this. Introducing stacked micro-vias and very short z-axis pathways will further reduce discontinuities and improve the PDN design.

Package solutions need to be developed and implemented that will deliver cleaner power to the IC, provide enough I/O to accommodate the volume of high speed SERDES and

increased functionality/bandwidth without compromising reliability and cost. Furthermore, the solutions must be compatible with current PCB design rules and component assembly processes.

Coreless substrate based semiconductor packages have been shown to significantly improve power integrity in network ASIC applications. Overall reliability and manufacturability was also shown as acceptable [1]. Coreless substrates offer designers flexibility in design, shortened pathways and are inherently very thin; these attributes can reduce package loop inductance and improve the overall power integrity of the package [2]. The issue with coreless based packages has always been that they are just not big enough to accommodate the next generation ASIC package. And, as they invariably must get larger to meet industry needs, both substrate warpage and resultant package warpage become marginal; complicating the manufacturability of the final product.

This paper discusses the benefits and compromises of using a coreless substrate-based Mixed Pitch Ball Grid Array (mpBGA) package with BGA-side capacitors. The component assembly flow and assembly optimization procedure is described along with L1 reliability data and PCB assembly/design rule considerations. Certain coreless substrate warpage mitigation techniques and efforts/challenges to model and simulate coreless warpage will be described.

Coreless mpBGA Test Vehicle Design

In the daisy chain Test Vehicle (TV) used in this paper, a variable 0.94mm pitch design is adopted to maximize the amount of I/O while also providing space for BGA-side capacitors. Since the challenge with coreless has always been not enough I/O at 1mm BGA pitch to meet existing network ASIC needs, mpBGA offers the opportunity for more routing at a manageable component body size. [3] In previous work, incorporating BGA-side capacitors has been shown to significantly improve the power delivery network in high speed ASIC designs [1,2]; however, one very significant compromise is that ball count had to be reduced to accommodate placing the capacitors (~1.6 balls/per back-side 0204 cap placed) [1]. Proper use of mpBGA results in an overall increase of ball count (especially for larger packages) and allows for BGA-capacitor placement. If added functionality, such as BGA-side capacitors is not required, mpBGA mitigates package size growth by providing more I/O per unit area. Maintaining coreless package sizes <50x50mm reduces L1/L2 reliability risk and package/PCB level assembly concerns and maintains a lower cost basis for the component.

A daisy chain TV was designed using a low ELK (40nm) 18mm x 22mm daisy chain silicon die. The 40nm Si was procured in two metallization schemes: 2MZ stack and 4MZ stack; DOE's were set-up around each stack to assess any differences in package assembly or reliability performance.

The coreless substrate is 45x45mm, 8+1 stack-up using GZ-41 - low CTE build-up material. The packages were designed with 0.5mm solder pad opening using 0.63mm SAC 305 BGA balls. The coreless packages were fabricated using a two-piece lid configuration. Two slightly different design variations were tested which varied the layer-to-layer copper distribution. Additionally, a variation of substrate material combinations that included combinations of solder resist (SR: SR-1 and SR-2) and build-up (BU) material (BU: BU-1 and BU-2) were tried as part of this development activity to assess and characterize warpage. Figure 1 shows the stack-combinations that were tested. All inner-layers were fabricated using BU-1 (BU-1 is GZ-41) whereas the outer-layers were varied with either another layer of BU-1 or a different material, BU-2 in order to test warpage mitigation strategies. Similarly, SR-1 and SR-2 were introduced for further warpage mitigation. The overall thickness of the multi-layer substrate was held at 0.390mm in all cases and the daisy chain interconnect was always consistent.

Design		1		2	
Layer	Thickness [µm]	Stackup 1	Stackup 2	Stackup 3	Stackup 4
1F	15	Cu			
1F-2F	20	BU-1	BU-2	BU-1	BU-2
2F	15	Cu			
2F-3F	30	BU-1			
3F	15	Cu			
3F-4F	30	BU-1			
4F	15	Cu			
4F-5F	30	BU-1			
5F	15	Cu			
5F-6F	30	BU-1			
6F	15	Cu			
6F-7F	30	BU-1			
7F	15	Cu			
7F-8F	30	BU-1			
8F	15	Cu			
8F-9F	30	BU-1			
9F	15	Cu			
BSR	25	SR-1		SR-2	
Total thickness	390				

Figure 1: Coreless substrate stack-up configurations.

Figure 2 shows the preferred mpBGA configuration. Twenty-eight 0204 (1µF) capacitors were placed on the back-side of the package directly under the die perimeter; forming a defacto separation between the “core-power” area and the “perimeter” outside the die shadow. The BGA-capacitors define a transition zone between two pitch configurations: the die perimeter using a 0.94mm orthogonal pitch, and the core-power area using a 1.0 mm hexagonal (interstitial) pitch.

In previous work [1], capacitors were placed directly under the die. L1 and L2 reliability testing was very good as were other critical parameters such as warpage, assembly yield and capacitor stand-off height (gap between capacitor on top of the PCB was shown to be typically 2-4 mils for 0204 capacitors with a nominal height of 0.3+/-0.05mm). In this iteration, placing the capacitors directly under the die perimeter was chosen because it is believed to be the highest

L2-interconnect stress zone. Determining the reliability impact removing BGA balls (from under the die perimeter area) will have on the adjacent BGA balls is essential in understanding how far BGA-capacitors can be placed away from the zero-stress point (center). Furthermore, this area may be important for placing AC-coupling caps on SERDES channels and thereby assessing the stress exhibited onto the capacitors (and solder joints) in this area is also critical; unlike decoupling caps which can in many cases be redundant so failures are not noticeable, AC-coupling capacitors cannot tolerate failures.

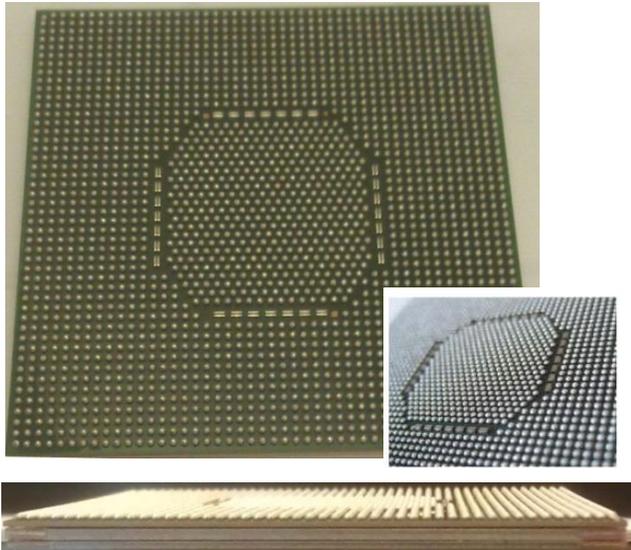


Figure 2: Top image illustrates BGA ball configuration with BGA caps. Bottom image is edge view showing 2-piece lid configuration and substrate (45x45mm package).

Figure 3 shows critical zones which were defined and isolated for Board Level Reliability (BLR) monitoring. The L1 interconnect (flip-chip bumps) was divided into 6 zones: defined by the die perimeter, die corner and die center area. These zones were subsequently divided into smaller regions. For example, the nine most corner bumps are monitored independently as it is believed they are likely to be exposed to the highest level of stress. And, the perimeter, which is defined as the first 10 rows of 170 μm bump pitch, is divided to isolate failures from the 3 outermost rows (bump pitch is 340 μm beyond the first 10 rows).

The L2 interconnect (BGA-balls) is monitored in 5 critical zones: including corner balls (zone 1), package perimeter (zone 4), die perimeter (zone 2), core power area (zone 5) and the neutral zone (zone 3). BGA-capacitors are placed between balls located in zone 2; the daisy chain net captures BGA-balls immediately adjacent to the BGA-capacitors in order to assess the stress displacement as described previously.

The daisy chain TV also monitors the substrate. Various micro-via and PTH chain configurations were included within the design. A high density of micro-vias was placed

in die corners, die perimeter and package perimeter. The via stack for the coreless design is 2-3-3 or 3-2-3.

JEDEC standard package Level 1 (L1) reliability tests (preconditioning with MSL-4, uHAST, 1000hr HTS, and 1000TCB (-55°C-125°C) were performed. Level 2 (L2) board level reliability (BLR) testing consist of 3500 cycles ATC (0°C-100°C), mechanical bending per IPC 9702 and mechanical shock (at 100, 200 and 340 G's input pulse). A BLR test vehicle was designed as a 125 mil, 16-layer PCB board using Pb-free compatible materials and VIPPO copper. A variety of board lay-out configurations were used to assess compatibility of BGA-caps with VIPPO and define PCB design rules. At the time of writing this paper L2 testing for the coreless substrate based packages is just starting.

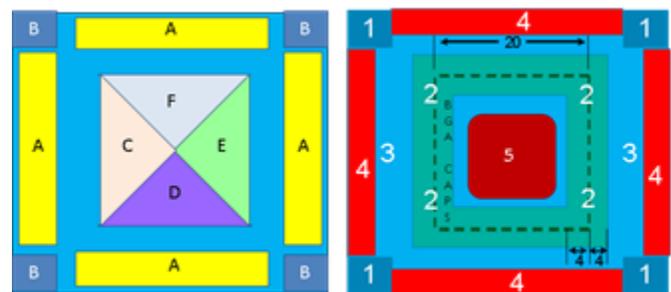


Figure 3: Left illustration shows L1 daisy chain zone definition (representing the die area: 18x22mm). Right illustration shows L2 zone configuration (representing the package area: 45x45mm).

Assembly Test Plan

Coreless Package Development Phases

There are many challenges in high end coreless, large die, large body flip chip package development. One of the major challenges is to keep the bare substrate flat to avoid non-wet or solder bridging issues during the flip chip assembly process. Unusually high warpage combined with CTE mismatch between the silicon and coreless substrate may exacerbate stresses in the ELK layers during the assembly leading to cracking or interlayer Si delamination. Other issues are controlling higher package warpage during printed circuit assembly reflow; solder bridging or opens may result if the package warpage is too high and there may be inherent stresses within the package which will impact the long-term board level reliability (BLR). The industry recognizes the important electrical advantages coreless substrates bring to high end ASIC applications and has evolved (and is currently developing) various methods to manage the warpage to within an acceptable window for high yielding assembly. [4,5,6]

Initial warpage measurements for the 45x45mm coreless substrate used in this study showed high warpage, especially at flip chip attach reflow temperature. A solution, utilizing a specialized Bill of Materials (BOM) and assembly warpage mitigation techniques, was developed to manage this warpage and has yielded good assembly results. Package

manufacturing conditions were characterized and optimized through several processes development phases as follows.

Step #1 (Thermo-mechanical simulation): Modeling and simulation was used to understand the package interactions during assembly and post reliability conditions. Numerical analysis helped down-select available substrate and package BOM sets and aided in defining the manufacturing/assembly DOE (Design of Experiment). Key driving force for this analysis was to identify which substrate configuration (as shown in figure 1) and assembly BOM resulted in the lowest warpage during assembly.

Step #2 (Assembly feasibility build): One of the most critical phases in developing the coreless manufacturing process was the feasibility build which used the results of the numerical analysis to down-select a preferred BOM for assembly. At the feasibility stage the main goal is to run a small quantity of material through the production process in order to ascertain which BOM produces the highest assembly yield and provides the best final package coplanarity and warpage (the data is also used to validate the models). Several key methods such as pre-attached metal stiffener, magnetic boat carrier, and tape carrier were used to mitigate the substrate warpage during the chip attach process. At the feasibility stage these warpage mitigation techniques were combined with a subset of various substrate build-up configurations (reference Figure 1).

Table 1 shows the combinations of assembly BOM sets used throughout the various process development phases. The variables included underfill (UF), Thermal Interface Material (TIM) and lid seal (LS) as well as the substrate design variations and silicon metal thickness. The subset of Table 1 used specifically during the Feasibility phase included *substrate types* from Legs 1, 5, 6 and 7. Varying and characterizing the UF's, TIM's and LS's were executed during the Characterization phase of this coreless assembly process development work (Step #3).

Table 1: Characterization Builds DOE

Leg#	Substrate type	Wafer type	Underfill	Lid Seal	TIM
1	Control (SR-1+BU-1)	4XMZ	UF-A	LS-A	TIM-A
2			UF-A	LS-A	TIM-B
3			UF-A	LS-B	TIM-A
4			UF-B	LS-A	TIM-A
5	SR-2+BU-1		UF-A	LS-A	TIM-A
6	SR1+BU-2		UF-A	LS-A	TIM-A
7	SR-2+BU-2		UF-A	LS-A	TIM-A

Figure 4 shows the coreless substrate warpage over temperature when employing the various assembly warpage mitigation techniques. The data is for the substrate type shown in Leg 1 (as defined in Table 1) but the trends are similar (or worse) for other substrate types. Very high warpage was observed with the bare substrate with “no-support” during assembly. Some improvement was

observed using the magnetic boat fixture and tape carrier but the warpage was still too large at higher temperatures for both these options to guarantee good yield. The lowest level of warpage was achieved using a pre-attached metal stiffener.

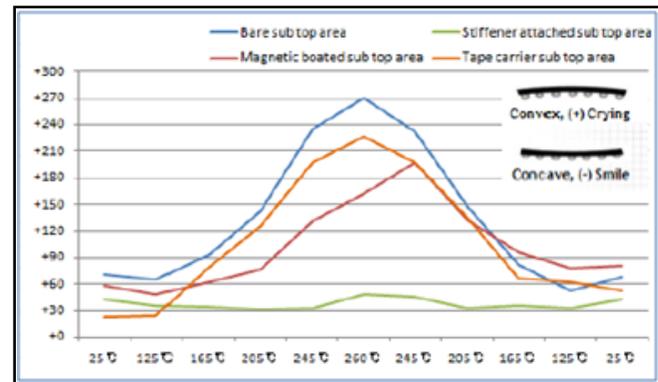


Figure 4: Coreless substrate warpage using different mitigation options during assembly. Lowest warpage observed with stiffener/highest warpage on bare substrate.

The expectation was that the lower CTE BU-1 would result in lower warpage since the CTE mismatch between the copper inner-layers, μ -vias and stiffener was better matched. The lowest warpage was found with BU-1 and SR-1 which confirmed the general expectation. This substrate material set was subsequently defined as the “control”. Bump bridging was observed with all the material combinations tested, except the control. The bump bridging was primarily due to higher concave warpage at the die corner locations even when using a pre-attached stiffener. Solder bump bridges and locations are shown in Figure 5. No solder bump bridge was observed with the control (Figure 6). The magnetic boat, tape carrier and bare substrate (no-support) also exhibited severe solder non-wetting in the corners as shown in Figure 7 for all substrate types except the control with metal stiffener.

Step #3 (Characterization build): At this point of the coreless assembly process development, the die UBM and passivation, substrate material type, lid design type / warpage mitigation technique (i.e. stiffener) were fixed. Additional testing and optimization of the TIM, UF and LS was required along with placement of the BGA-side capacitors. The “best” process was determined by running reliability testing (MSL-4 preconditioning, un-biased HAST, HTS, and 1000TCB) on an abridged sample size (~20 units) and characterizing the final package warpage and lid adhesion (not all this data will be shown in this paper).

TIM-B, UF-B and LS-B variables as shown in Table 1 were introduced to gauge their effect on typical L1 assembly defects associated with large package/large die ELK-Si (i.e. white bump, bump crack, low-k delamination) and overall package co-planarity and warpage. The low CTE BU-1

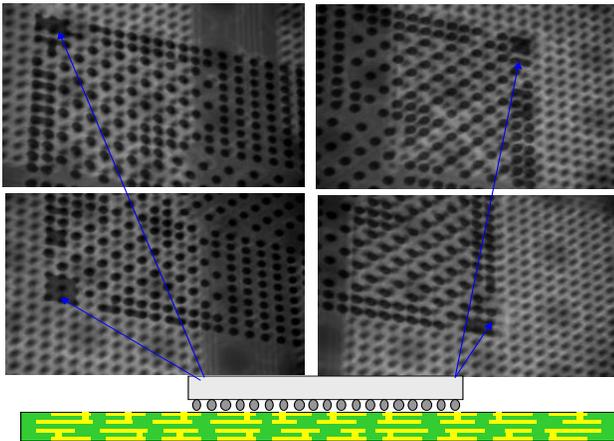


Figure 5: Typical bump bridging picture and locations

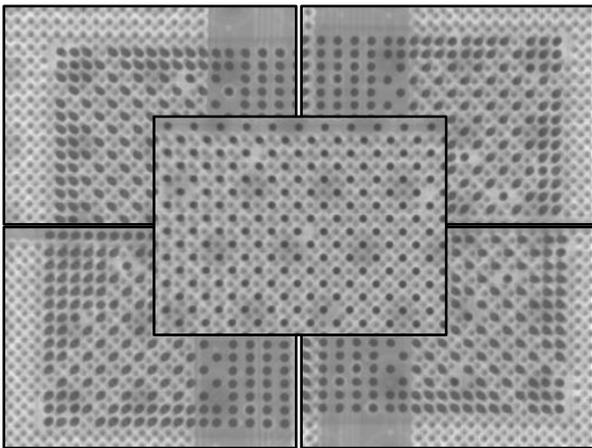


Figure 6: No bump bridge (or other L1 interconnect anomaly) w/ control substrate type.



Figure 7: Examples of severe non-wet w/ coreless substrate using magnetic boat, and tape carrier on all substrate types except “control”

with SR-1 (aka “control”) had already shown to provide a better substrate warpage during the flip-chip attach and it was believed that it would also mitigate occurrences of “white bumps”. The 40nm silicon that was used during the characterization build phase incorporated a thicker metallization scheme (4MZ) but previous work [3] showed very little difference between the “robustness” of the

various metal layer thicknesses as applied to large body thin core packages.

The two different underfill materials varied in Tg (glass transition temperature). The high Tg underfill (UF-B) is recommended to protect the Pb-free bump whereas low Tg (UF-A) is for better ELK protection and package warpage control. Selecting the right underfill type for a large coreless package with ELK die is very challenging and requires delicate compromise.

High thermal conductive TIM was required because of the high-end ASIC package and expected thermal dissipation requirement (>100W) for such devices. Two high conductive TIMs along with 2 lid seal materials were tested. Both the TIM and lid adhesive materials were extensively characterized to meet certain requirements such as wider process window to dispense epoxy and attach lid, higher lid-pull strength, low thermal resistance, etc. TIM-B is manufactured with highly filled Ag particle resulting in higher thermal and higher stiffness material over soft gel type TIM-A. Warpage data shows that legs using the “control” substrate type comfortably met the “end of line” (EOL) metric for package warpage (< 200µm) whereas other legs did not. Lid pull tests were performed at EOL for all lid adhesives and TIM combinations. Eventhough all legs passed the lid pull test criteria (195Kgf at 25°C), only TIM-B and LS-A were selected as part of the “preferred BOM” due to better processability and higher bulk thermal conductivity of TIM-B.

One of the key design features of this study is the incorporation of the BGA-side mounted capacitors onto the 8+1 coreless substrate. No process had heretofore been developed to conduct such an assembly on multi-layer coreless. Several iterations of the design and assembly process were performed to finalize the process window. A typical coreless package assembly process was applied in the study as shown in Figure 8.

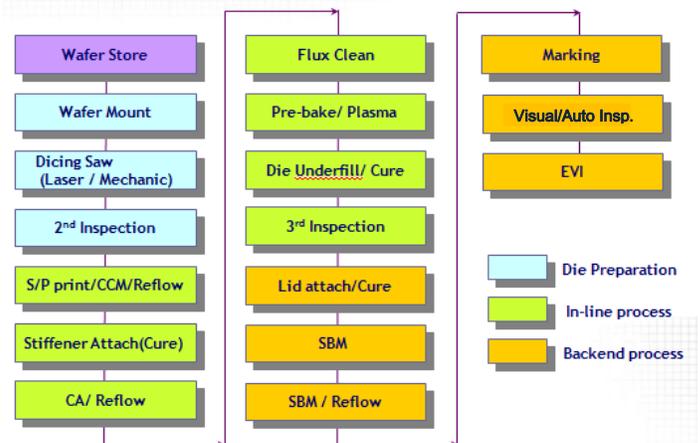


Figure 8: Typical assembly process flow for Coreless FC with BGA side capacitors.

A check list for various process steps during assembly was developed and monitored during the assembly process to ensure it met all required conditions. The detailed check list with monitoring methodologies is shown in Table 2.

Table 2: Check list and “passing” criteria for coreless packages produced during Characterization phase.

Process	Check Items	Criteria	Methodology
LID Attach	Alignment	Max. 200um alignment	Vertical gauge measurement for X, Y Diameter, Tilt
	Adhesive coverage	Depend on foot width of Lid	Lid detach after Adhesive dispense
	TIM coverage	Min. 90% of die area	Lid detach after TIM dispense
	Lid pull test	Min. 19.5kgf @25C	Lid pull test after cure
	Warpage	Max. 200um	Shadow Moir'e measurement
Solder/paste print	Missing print	Not allowed missing print	Visual Inspection during Assembly
SMT	Paste wetting	. Min. 50% fillet height . Not allowed tombstoning, Misplacement	Paste quality, Composition, Misplacement, Tombstoning
Solder ball mount	Ball missing, Bridge, Misplacement, Coplanarity	. Not allowed missing, bridge, misplacement ball . Max. 200um	Visual or Auto Inspection
	Ball shear test	Min. 500g	Ball shear tester
	Clearance between solder ball and BGA side Chip cap.	No interference between chip cap. and solder ball	Visual & Optical Inspection
	Warpage	Max. 200um	Shadow Moir'e measurement
Final visual inspection	POD compliance		POD Compliance

Electrical open short (O/S) tests were performed after each accelerated reliability test condition. Any failed units were cross-sectioned to verify failure results and failure mode. Post reliability data shows UF-A slightly outperformed UF-B, hence it was selected for the qualification build.

Significantly lower package warpage at all temperatures were observed with the combination of BU-1, UF-A, LS-A, and TIM-B combination. Figure 9 shows EOL package warpage plot over temperatures with TIM types.

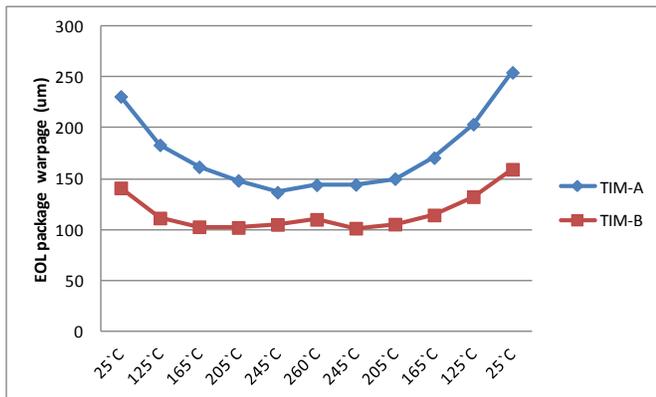


Figure 9: EOL package warpage over all temperature using TIM-A, and TIM-B. TIM-B -Red curve (Bottom curve) represents preferred BOM.

Upon completion of comprehensive JEDEC L1 package reliability tests, no visible or electrically tested anomalies were noticed with leg#2 BOM; therefore, it was selected as

the “preferred” BOM for final validation and full sample size/ multi-lot package qualification.

Step #4 (Package and Board level qualification): The final step of development is the qualification build where only the best leg from the characterization step (STEP 3) was selected for comprehensive package and board level reliability (full samples size/multiple build lots). Once comprehensive reliability testing is completed on the qualification build samples (and samples have passed), the process will be ready to scale to high volume manufacturing. Typical reliability read-points for the qualification build were EOL (End of Line) X-ray inspection, C-mode scanning (CSAM) to check for any voids, delamination or other abnormalities during assembly and accelerated test conditions, and package warpage as a function of temperature. Electrical open short testing was performed after each test item using a dedicated high volume, fully automated, test socket. Extensive failure analysis was also conducted to monitor material interface delamination, cracking, or any other abnormalities in the package.

The qualification and validation build consisted of 135 samples assembled using Leg 2 BOM. The units were subjected to JEDEC standard comprehensive reliability tests as shown in Table 3. Packages were built in 3 different lots each with 45 units. No issues were encountered in the package assembly process for any of the 3 sub-lots. CSAM results were taken on every part after the underfill cure process to make sure no voiding or delamination occurred in the packages.

Table 3: Package level qualification builds DOE

sample size	EOL package warpage	precon L4	uHAST		HTST (150C)		TCB (-55 to 125C)	
			96 hours	168 hours	500 hours	1000 hours	500 cycles	1000 cycles
135	3	105	30	28	30	28	73	71

All units comfortably passed the reliability tests. TCB parts were extended to 1000X cycle to check the bump integrity. No anomaly was observed through 1000X shown in Figure 10 (testing was extending to 2000X for information only and also passed). The package level post reliability requirements were kept the same in the qualification build (JEDEC standard package level reliability tests: preconditioning with MSL-4, uHAST, HTS, and TCB). Again, electrical open short tests were performed on every part after every read-point. No failure or other degradation was observed in any of the samples. Table 4 shows complete reliability data of qualification build parts. CSAM pictures were also taken on a few parts after each reliability tests; no failures were detected.

EOL condition package warpage data that was collected using Shadow Moiré package warpage is within specification (<200um) at any given temperature condition. The warpage trend follows smile-to-crying as packages go from room temperature to elevated temperatures. Warpage is shown in Figure 11

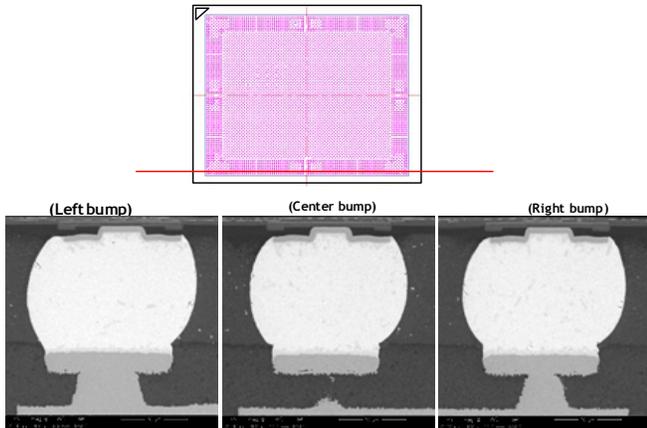


Figure 10: Cross-section of flip chip bumps across the width of the package. No bump anomalies (or other failures modes) noticed through TCB 1000.

Extensive failure analysis is being conducted on post reliability parts to look for bump cracks or other oddities in the package as a result of the various standard tests. All data collected to-date suggests that an assembly process using a pre-attached metal stiffener is capable of producing a high yielding and reliable large die, 45mm X 45mm coreless package with mpBGA and BGA-side capacitors. L2 testing is planned to further substantiate the robustness of the packing solution.

Table 4: Qualification build parts reliability data

EOL	precon L4	uHAST		HTST (150C)		TCB (-55 to 125C)	
		96 hours	168 hours	500 hours	1000 hours	500 cycles	1000 cycles
O/S test	O/S test	O/S test	O/S test	O/S test	O/S test	O/S test	O/S test
0/135	0/105	0/30	0/28	0/30	0/28	0/73	0/71

PCB Considerations for use of coreless mpBGA

Impact of mpBGA on PCB routing requires additional consideration in order to maintain high yielding PCB manufacturability. Implicit in the 0.94 mm pitch design is that escape routing for high-end network system applications will still require two tracks between pins on signal layers and that copper webs between pins on plane layers will not be reduced. This means that registration is more challenging than it is with standard 1 mm pitch designs. [3]

Smaller plated through holes (PTH's) are required and may have an inherent improvement in SI but will approach the

PCB manufacturer's current capability. Changes to anti-pads may be required but if hole size can be small enough and registration can be maintained, it would have little overall impact on PCB lay-out (or SI). VIPPO copper will simplify the PCB routing and registration challenges (and improve SI) somewhat but comes with a slight premium in cost. An additional consideration when using mpBGA is that signal layer routing within the BGA footprint is more complicated, especially so when signal traces must transit the hexagonal pin arrangement in the power core. It is possible that routing efficiency will be lower relative to the standard 1 mm orthogonal arrangement, and in limiting cases may require that additional signal layers be added to the design.

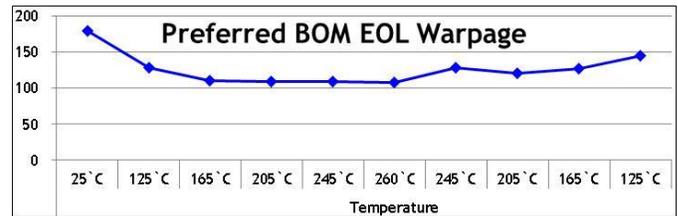


Figure 11: Package warpage for the Preferred BOM

Previous work using 40mm x 40mm coreless substrates demonstrated that warpage of a coreless-based substrate packages is generally flat at component reflow conditions [1]. This phenomenon can also be seen in the Figure 12 for the 45mm x 45mm. Warpage during PC assembly is even more critical for coreless-based packages with BGA-side capacitors. Previous work showed that the capacitors generally do not “touch” the surface of the PCB during assembly for large body thin core (0.4mm) applications [1,3]; however, this has yet to be demonstrated for the coreless configuration.

Warpage Mitigation

As highlighted numerous times within this paper, warpage of the coreless substrate is a significant hurdle that must be overcome for successful implementation of large body coreless substrates. The techniques discussed in this paper effectively “manage” the warpage through the assembly process. Other techniques have been developed to manage the warpage using specialized tooling [5], novel soldering techniques [4] or heat pre-treatment [6].

The goal, however, is to eliminate warpage with proper design and material combinations that behave in a predictable manner through the various manufacturing/assembly steps and product life-cycle. Throughout the course of this development activity a major goal was to develop models that can effectively predict the behavior of the substrates based on the substrate materials and design such that design tweaks can be incorporated early and eliminate warpage. In this study various coreless build-up material combinations were tested-including mixed-material combinations. Two designs were generated with slightly different copper balancing distribution. Models

to predict room and high temperature co-planarity for thin-core solutions were previously developed and showed good correlation [7]. These techniques were refined for various coreless configurations and samples were fabricated to correlate and validate the simulation results. Figure 12 shows a comparison of the actual measured warpage for a specific build-up configuration and the predicted modeling values. The trends are captured reasonably well but considerable more work is required to properly capture variability in processing and subtle design and materials changes. Moreover, the modeling and simulation work needs to be extended into predicting performance at the final package level.

Future work will focus on establishing a fundamental understanding of the visco-elastic properties of the materials and the impact substrate manufacturing variations may have on the final substrate material properties.

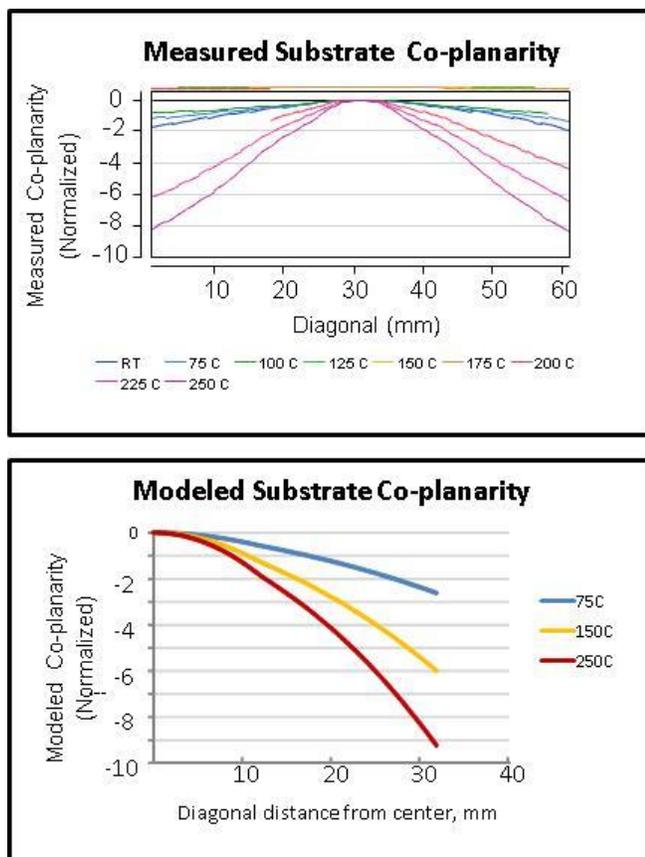


Figure 12: [Top] Measured coplanarity over temp for a test sample multi-layer coreless substrate. [BOT] Predicted substrate co-planarity for a test sample multi-layer coreless substrate. Graph demonstrates trend correlation.

Conclusions

The coreless mpBGA reliability and manufacturability evaluation has shown that a 45 x 45mm coreless substrate package with large body ELK silicon die and BGA-side

capacitors is robust for assembly and performs exceptionally well through critical JEDEC level reliability testing. Eventhough incoming co-planarity of the coreless substrate was marginal, the warpage was mitigated well-enough through the use of a stiffener and a well-defined assembly BOM. The preferred BOM and manufacturing process produced high quality test vehicles with very high yield.

More work is required in developing tools to effectively model and predict the performance of the coreless based substrates-particularly for next generation materials and even larger body sizes.

mpBGA coreless substrate-based packages with BGA-side capacitance effectively placate both the functional and economic requirements confronting next generation high speed network packaging solutions by enabling higher levels of functionality at sustainable body sizes, while concurrently delivering exceptional reliability and high yielding manufacturability.

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